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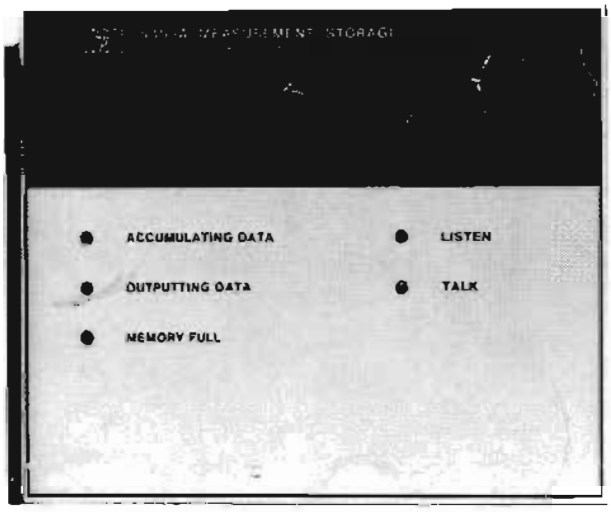
（例：旧製品名 HP 8648は、現在 Agilent 8648として販売いたしております。）

Agilent Technologies

OPERATING AND SERVICE MANUAL

MEASUREMENT STORAGE PLUG-IN

5358A



HEWLETT hp PACKARD

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HEWLETT hp PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this instrument met its published specifications at the time of shipment from the factory. Hewlett-Packard Company further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY AND ASSISTANCE

This Hewlett-Packard product is warranted against defects in materials and workmanship for a period of one year from the date of shipment. Hewlett-Packard will, at its option, repair or replace products which prove to be defective during the warranty period provided they are returned to Hewlett-Packard, and provided the preventive maintenance procedures in this manual are followed. Repairs necessitated by misuse of the product are not covered by this warranty. NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

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5358A
MEASUREMENT STORAGE PLUG-IN

OPERATING AND SERVICE MANUAL

SERIAL PREFIX: 1628A AND 1640A

This manual applies to Serial Prefix 1628A and 1640A, unless accompanied by a Manual Change Sheet indicating otherwise.

MANUAL PART NUMBER 05358-90004
Microfiche Part Number 05358-90005

Printed: NOV 1977

HEWLETT hp PACKARD

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SAFETY CONSIDERATIONS

GENERAL

This is a Safety Class I instrument. This instrument has been designed and tested according to IEC Publication 348, "Safety Requirements for Electronic Measuring Apparatus."

OPERATION

BEFORE APPLYING POWER verify that the 5345A power transformer primary is matched to the available line voltage and the correct fuse is installed (see Section II). Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.

SERVICE

Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service and adjustments should be performed only by qualified service personnel.

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

WARNING

IF THIS INSTRUMENT IS TO BE ENERGIZED VIA AN AUTOTRANSFORMER (FOR VOLTAGE REDUCTION) MAKE SURE THE COMMON TERMINAL IS CONNECTED TO THE EARTHED POLE OF THE POWER SOURCE.

WARNING

BEFORE SWITCHING ON THE INSTRUMENT, THE PROTECTIVE EARTH TERMINALS OF THE INSTRUMENT MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE (MAINS) POWER CORD. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE CONDUCTOR (GROUNDING).

WARNING

THE SERVICE INFORMATION FOUND IN THIS MANUAL IS OFTEN USED WITH POWER SUPPLIED AND PROTECTIVE COVERS REMOVED FROM THE INSTRUMENT. ENERGY AVAILABLE AT MANY POINTS MAY, IF CONTACTED, RESULT IN PERSONAL INJURY.

CAUTION

BEFORE SWITCHING ON THIS INSTRUMENT:

1. MAKE SURE THE INSTRUMENT IS SET TO THE VOLTAGE OF THE POWER SOURCE.
2. ENSURE THAT ALL DEVICES CONNECTED TO THIS INSTRUMENT ARE CONNECTED TO THE PROTECTIVE (EARTH) GROUND.
3. ENSURE THAT THE LINE POWER (MAINS) PLUG IS CONNECTED TO A THREE-CONDUCTOR LINE POWER OUTLET THAT HAS A PROTECTIVE (EARTH) GROUND. (GROUNDING ONE CONDUCTOR OF A TWO-CONDUCTOR OUTLET IS NOT SUFFICIENT.)
4. MAKE SURE THAT ONLY FUSES WITH THE REQUIRED RATED CURRENT AND OF THE SPECIFIED TYPE (NORMAL BLOW, TIME DELAY, ETC.) ARE USED FOR REPLACEMENT. THE USE OF REPAIRED FUSES AND THE SHORT-CIRCUITING OF FUSE HOLDERS MUST BE AVOIDED.

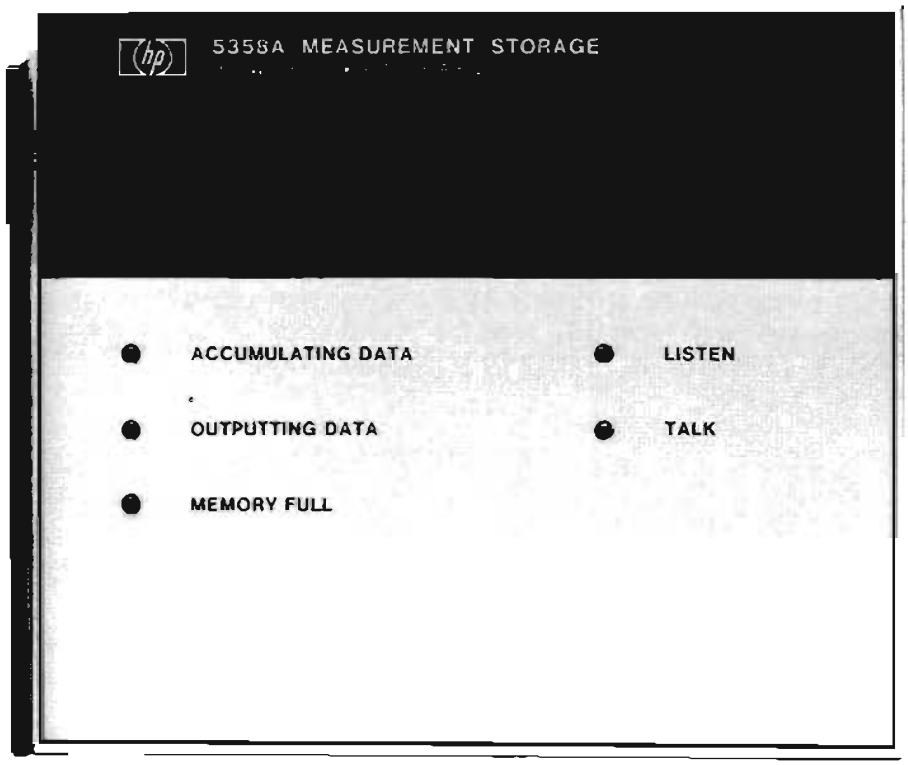


Figure 1-1. Model 5358A Measurement Storage Plug-In

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This manual provides information pertaining to the installation, operation, testing, adjustment and maintenance of the HP Model 5358A Measurement Storage plug-in unit.

1-3. *Figure 1-1* shows the HP 5358A which is a plug-in unit for the HP 5345A Electronic Counter.

1-4. SPECIFICATIONS

1-5. Instrument specifications are listed in *Table 1-1*. These specifications are the performance standards or limits against which the instrument may be tested. Specifications are based on operation with the HP 5345A Electronic Counter (with Option 011) of serial prefix 1624A or later and a Hewlett-Packard Interface Bus (HP-IB) compatible controller (i.e., 9825A). *Table 1-2* lists the operational characteristics of the 5358A.

1-6. INSTRUMENTS COVERED BY MANUAL

1-7. This instrument has a two-part serial number. The first four digits and the letter comprise the serial number prefix. The last five digits form the sequential suffix that is unique to each instrument. The contents of this manual apply directly to instruments having the same serial number prefix(es) as listed under SERIAL PREFIX on the title page.

1-8. An instrument manufactured after the printing of this manual may have a serial prefix that is not listed on the title page. This unlisted serial prefix indicates that the instrument is different from those documented in this manual. The manual for this instrument is supplied with a yellow Manual Changes supplement that contains change information that documents the differences.

Table 1-1. Model 5358A Specifications

EXTERNAL TRIGGER INPUT

Trigger Slope: Program selectable, transition either logic 0 to 1 or 1 to 0.
Connection: Rear panel BNC labeled ACCUM TRIG IN.
Electrical: Section of rear panel address switch marked Y selects either TTL (4-volt) or 50 ohm (1-volt) load input as follows:
Logic 1: +2.4V (min) TTL load
+0.8V (min) 50 ohm load
Logic 0: +0.8V (max) TTL load
+0.2V (max) 50 ohm load
Pulse Width: Greater than or equal to 100 ns.

MEASUREMENT TIME SIGNAL OUTPUT

Connector: Rear panel BNC labeled SAMPLE TIME MEAS OUT and DEAD OUT (complementary outputs).
Electrical:
Logic 1: -1.5V ±0.5V (into 50Ω)
Logic 0: 0V ±0.1V (into 50Ω)

EXTERNAL DEAD TIME GENERATOR INPUT/OUTPUT

Dead Time Start Output:
Trigger Slope: Program selectable, transition either logic 0 to 1 or 1 to 0.
Connector: Rear panel BNC labeled DEAD TIME START OUT.
Electrical: (TTL output to TTL load, or 0 to 1 volt output to 50 ohm load)
Logic 1: +2.4V (min) TTL load
+0.8V (min) 50 ohm load
Logic 0: +0.8V (max) TTL load
+0.2V (max) 50 ohm load
Pulse Width: Greater than than or equal to 100 ns.

Dead Time Stop Input:
Trigger Slope: Program selectable, transition either logic 0 to 1 or 1 to 0.
Connector: Rear panel BNC labeled DEAD TIME STOP IN.
Electrical: (TTL input)
Logic 1: +2.4V (min)
Logic 0: +0.8V (max)

Table 1-2. Operational Characteristics

MEMORY SIZE

Standard: 2048 bytes.
Optional: 4096, 6144, or 8192 bytes

MEASUREMENT CONTROL

Data Accumulation Modes:
- Continuous: Continuously stores measurement data between commands.
- Counted: Accumulates N measurements, stops, and signals completion.

Gate Mode:
- Not Hold: Gate free runs
- Hold: Gate is held off until data accumulate command.

Measurement Count: N is program selectable in the range between 1 and 9999.
Data Accumulation Command:
May be initiated by:
1. HP-IB Program Code
2. HP-IB Device Trigger Function (GET)
3. External Trigger.

Measurement Time:
- Range: 1 to 999 x 10^8 μs
- Resolution: 3 digits (for gate time >100 μs and 1 μs for gate time ≤100 μs)

Dead Time:
- Minimum Mode: Less than 7 μs plus 2 μs for each digit transferred from 5345A to 5358A.
- Ratio Mode: Ratio of measurement time to dead time selectable as either 2:1 or 1:1.
- External Mode: External timer such as HP 59308A Timing Generator may be used to program dead time.

DATA CONTROL

Digits Transferred: Range from 1 to 13. Each measurement digit requires 1 byte of memory storage.
Output Formats:
1. ASCII Format <time scaler>, <events scaler> (CR) (LR) .
2. Packed BCD, most significant digit first, 2 digits per byte.
3. Binary Format (first in first out).

OPERATIONAL AIDS

HP-IB Status Byte: Provides indication via HP-IB of the status of the 5358A.
Information provided:
- STB1: Power down at some previous time.
- STB2: Real Dead Time exceeded the programmed Dead Time.
- STB3: Attempt was made to store data when memory was full.
- STB4: Memory Status 0 0 Empty
- STB5: Memory Status 0 1 ≤½ full
- 1 0 >½ full
- 1 1 Full
- STB6: Counted (N) measurements have been completed
- STB7: Indicates service is requested.

Service Request: Service is requested by any of the following conditions.
1. Power up/down condition
2. Real dead time > programmed dead time
3. Counted (N) measurements completed
4. Memory full.

Front Panel Indicators:
- ACCUMULATING DATA: Indicates 5358A is actually accumulating data
- OUTPUTTING DATA: Indicates 5358A is outputting data to the HP-IB interface
- MEMORY FULL: Main memory is full and accumulation of data is stopped
- LISTEN: The 5358A is ready to accept program instruction or data from the HP-IB interface
- TALK: The 5358A is ready to output data to the HP-IB interface.

Rear Panel BNC Connectors:
- ACCUM TRIG (in): Input for external trigger
- SAMPLE TIME
  - $\overline{\text{MEAS}}$ (OUT): Output external gate for 5345A
  - DEAD (OUT): Output external gate for 2nd 5345A (complementary to $\overline{\text{MEAS}}$)
- DEAD TIME:
  - START (OUT): Output trigger for timer to start dead time
  - STOP (IN): Input from timer to stop dead time.

1-9. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the last Manual Changes supplement. The supplement for this manual is keyed to the manual's print date and part number, both of which appear on the title page. Complimentary copies of the supplement are available from Hewlett-Parkard.

1-10. For information concerning a serial number prefix not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

1-11. DESCRIPTION

1-12. The HP 5358A plug-in (for the HP 5345A Electronic Counter) stores measurement information at a rapid rate for later retrieval and processing at a slower transfer rate via the Hewlett-Packard Interface Bus (HP-IB). The plug-in also generates precise measurement gating signals for the 5345A under control of the HP-IB.

1-13. The measurement storage capability of the plug-in, and fast data transfer from the counter, allow measurements to be taken with minimal dead time (nonmeasurement time) between measurements. The data consists of time and event scaler information from the 5345A and can be processed by either a calculator or a computer which is equipped with HP-IB capability. A FREE RUN (or "talk only") switch (marked X) is provided on the rear panel of the plug-in to allow HP-IB compatible instruments to retrieve the stored data without having to program either the counter or the plug-in.

1-14. Programming of both the counter and plug-in via the HP-IB allows the counter (with HP-IB Option 011) to be programmed for maximum sample rate while the plug-in can be programmed for the number of data digits required to be transferred, to provide fast measurements. Other programming features include initiating a sequence of measurements on command, presetting the number of measurements to be made, and placing the counter into a "HOLD" condition until an initiating command or external trigger is activated.

1-15. The gate signal generator in the 5358A is provided to generate a programmable gate signal for precise control of the counter's measurement and dead time. Programming codes specify the gate signal (measurement time) in terms of a mantissa (3 digits) and exponent (0—6) in microseconds. Dead time (nonmeasurement time) is program code selectable in terms of ratio to measurement time, minimum time, or externally generated time such as provided by the HP 59308A Timing Generator.

1-16. The plug-in incorporates HP-IB service request and serial poll features. The status byte indicates the occurrence of previous power failure, synchronizing errors, end-of-measurement series and memory status. These features are described in detail in Section III and VIII.

1-17. OPTIONS

1-18. The only option for the 5358A is Option 001. This option is a printed-circuit board that is identical to the A8 Memory board in the standard 5358A. Each board provides 2048 bytes of memory. A total of three Option 001 boards may be added to the standard 5358A to increase the memory from 2K to 8K.

1-19. EQUIPMENT REQUIRED BUT NOT SUPPLIED

1-20. To have a complete operating measurement storage unit, the HP Model 5358A Measurement Storage Plug-In must be installed in an HP Model 5345A Electronic Counter mainframe with Option 011. Mainframes with serial prefixes 1624A and above need no modification. There must also be an HP-IB compatible controller for programming, and retrieval of stored data.

1-21. There are two accessories needed which are not supplied. The first is a 12-inch coaxial BNC cable, HP Part Number 11170A; and the second is a ½-meter length HP-IB interconnect cable, HP Part Number 10631D.

1-22. EQUIPMENT AVAILABLE

1-23. A data tape cartridge with 5358A Diagnostic Program HP Part Number 05358-16000 is available for convenience in troubleshooting the 5358A Plug-In. The tape cartridge is used with an HP Model 9825A Desk Top Controller and an HP 9871A or 9866B Printer. A Diagnostics Special Function Key overlay HP Part Number 05390-80001 is available for the HP 9825A as an aid for convenient use of the Special Function keys needed for effective troubleshooting.

1-24. RECOMMENDED TEST EQUIPMENT

1-25. Equipment required to maintain and troubleshoot the HP Model 5358A is listed in *Table 1-3*. Other equipment may be substituted if it meets or exceeds the required characteristics listed in *Table 1-3*.

1-26. APPLICATIONS

1-27. The 5358A in the 5345A Electronic Counter with Option 011 provides for accumulation of high-speed data in any one of the counter's five functions. Data can be retrieved either by a calculator/computer-based system or by the Free Run mode. In the calculator/computer-based system, the programmable gate signal can be used for externally gating the counter or for alternating measurement/data collection between two counters. Specific applications for the 5358A are as follows:

a. High-speed measurement storage and gating signal generation in systems such as the HP 5390A Frequency Stability Analyzer.
b. Data collection of time intervals separated by short duration deadtimes.
c. Data storage of counter measurements for later retrieval. This feature can be used in a data acquistion system in which the data is accessed at intervals.

Table 1-3. Recommended Test Equipment

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED
Electronic Counter	No substitute	HP 5345A Option 011
Controller	No substitute	HP 9825A Option 001
Printer		HP 9866B or HP 9871A
Oscilloscope	Storage	HP 184A
Vertical Amplifier	Four channel	HP 1809A
Time Base		HP 1825A
ROM	No substitute	HP 98210A
ROM	No substitute	HP 98214A
Interface		HP 98032A Option 066 for HP 9866B
Interface		HP 98034A for HP 9871A
Scope Probes	10:1 (four required)	HP 10014A
Logic Probe		HP 10525T
Logic Pulser		HP 546A
Current Tracer		HP 547A
Diagnostic Cartridge	5358A Diagnostic Software for HP 9825A	HP 05358-16000
Key Overlay	Special Function Key Overlay for HP 9825A	HP 05390-80001
Extender Board	2 x 22 4.5" Tall (two required)	HP 5060-0630
Extender Board	2 x 12 4.5" Tall	HP 5060-0258

SECTION II
INSTALLATION

2-1. INTRODUCTION

2-2. This section provides instructions for unpacking, inspection, preparation for use, storage, and shipment of the 5358A plug-in.

2-3. UNPACKING AND INSPECTION

2-4. If the shipping carton is damaged, inspect the 5358A for visible damage (scratches, dents, etc.). If the 5358A is damaged, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately (offices are listed at the back of this manual). Keep the shipping carton and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of your instrument without waiting for the claim against the carrier to be settled.

2-5. PREPARATION FOR USE

2-6. Power Requirements

2-7. The 5358A does not require external ac power. All necessary power is supplied by the 5345A when the 5358A is plugged in.

2-8. Operating Environment

2-9. The operating temperature range is 0°C to 40°C. If these limits are exceeded at the installation site, auxiliary cooling or heating should be used to keep environment within limits.

2-10. Installation

2-11. To install the 5358A, proceed as follows:

a. On the 5345A, set POWER switch to STANDBY.

b. Pull the locking handle on the left side of the 5358A up to the horizontal position.

c. Slide the 5358A into the 5345A.

d. Push locking handle down and toward the instrument until it is parallel with the front panel.

e. For operating information, address switch settings, and connections to rear panel BNC connectors, refer to Section III. If the 5358A is used in a 5390A Frequency Stability Analyzer System, refer to the 5390A System manual.

2-12. Compatibility with 5345A

2-13. The 5358A is compatible with 5345A's that have Serial Prefix 1624A or higher. If a 5358A is to be installed in a 5345A that has a serial prefix lower than 1624A, certain wiring and board changes must be made in the 5345A. Contact the nearest HP Sales and Service office (listed at the back of this manual) for information.

2-14. Operational Check

2-15. To determine if the instrument is operating properly, refer to the in-cabinet performance check in Section IV. Contact the nearest HP Sales and Service Office (see manual back cover) for information relative to warranty claims.

2-16. PACKAGING FOR RESHIPMENT

2-17. Original Packaging

2-18. The same containers and materials used in factory packing can be obtained through the Hewlett-Packard Sales and Service Offices listed at the rear of this manual. The HP part number for the shipping carton is listed under "MISCELLANEOUS" in *Table 6-1*.

2-19. If the instrument is being returned to Hewlett-Packard for service, attach a tag indicating the type of service required, return address, model number, and full serial number. Mark the container FRAGILE to assure careful handling.

2-20. In any correspondence refer to the instrument by model number and full serial number.

2-21. Other Packaging Methods

2-22. If it becomes necessary to reship an instrument, good commercial packing should be used. Contract packaging companies in many cities can provide dependable custom packaging on short notice. The following general instructions should be followed when repackaging with commercially available materials.

a. If shipping to a Hewlett-Packard Office or Center, attach a tag indicating the type of service required, return address, model number, and full serial number.

b. Wrap the instrument in heavy paper or plastic.

c. Use a strong shipping container. A double-wall carton made of 350-pound test material is adequate.

d. Use enough shock-absorbing material (3- to 4-inch layer) around all sides of the instrument to provide a firm cushion and prevent movement inside the container. Protect the control panel with carboard.

e. Seal the shipping container securely.

f. Mark the shipping container FRAGILE to assure careful handling.

2-23. STORAGE

2-24. If the instrument is to be stored for an extended period of time, it should be enclosed in a clean, sealed container.

SECTION III
OPERATION AND PROGRAMMING

3-1. INTRODUCTION

3-2. This section describes the operating characteristics and the front and rear panel features of the 5358A. Operating and programming information is also provided, including address switch settings and HP-IB program codes for the 5358A.

3-3. The 5358A is programmed via the Hewlett-Packard Interface Bus (HP-IB). The HP-IB is a carefully defined instrumentation interface which simplifies the integration of instruments, calculators, and computers into systems. For a brief description of the HP-IB refer to the "Condensed Description of the Hewlett-Packard Interface Bus" (P/N 59401-90030). HP-IB is Hewlett-Packard's implementation of IEEE Standard 488-1975, "Standard Digital Interface for Programmable Instrumentation."

3-4. The 5358A is a plug-in for the 5345A Electronic Counter (Option 011). Operating and programming characteristics of the 5345A must be understood before attempting to operate and program the 5358A. For complete information on the 5345A, refer to the 5345A Operating and Service Manual. When appropriate, the 5358A programming explanations that follow contain notes on the interrelated 5345A programming instructions. See also paragraph 3-18.

3-5. PANEL FEATURES

3-6. The function of front panel indicators and of the rear panel switch assembly and connectors is described in *Figure 3-1*.

3-7. OPERATING CHARACTERISTICS

3-8. The 5358A plug-in functions to accumulate high-speed data from the 5345A in any one of the counter's five functions (FREQ A, PERIOD A, TIME INT. A to B, RATIO B/A, and START). Data can be retrieved by a calculator or computer in a controller-based system. The programmable gate signal of the 5358A is used for precise control of the counter's measurement time.

3-9. The counter and the plug-in can be programmed via the HP-IB to provide optimum timing for measurements being taken. The counter can be programmed for maximum sample rate and the plug-in can be programmed for the minimum number of digits required to be transferred, to reduce the nonmeasurement time. In addition, the 5358A can be programmed to:

a. Initiate a sequence of measurements on command.

b. Preset the number of measurements to be made.

c. Place the counter in a "HOLD" condition until an initiating command or external trigger is activated.

d. Specify the gate signal (measurement time) in terms of a mantissa and exponent.

e. Select dead time (nonmeasurement time) in terms of:

   (1) Ratio to measurement time—

   (2) Minimum time—

   (3) Externally generated time (such as timing provided by an HP 59308A Timing Generator).

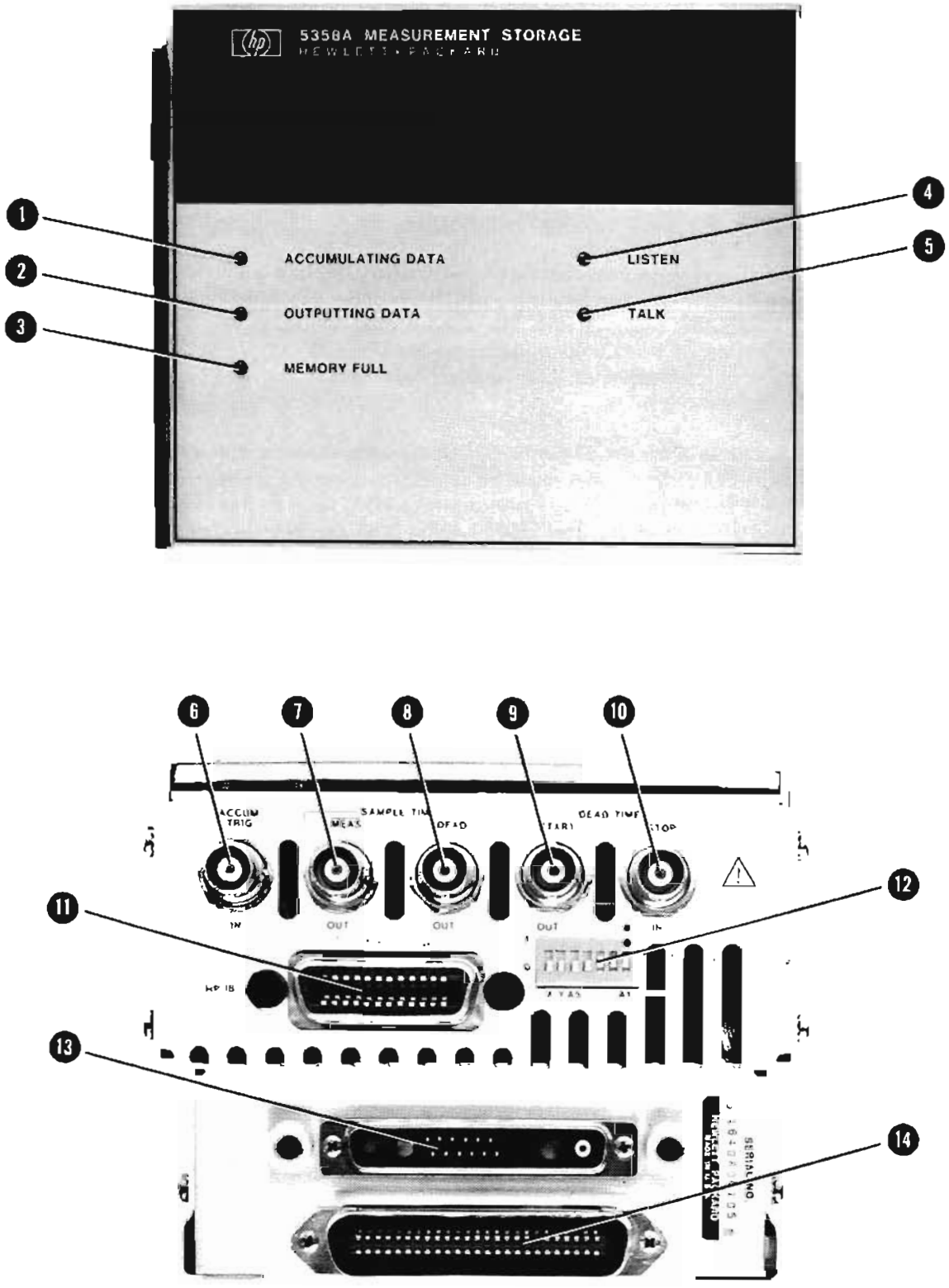


Figure 3-1. Front and Rear Panel Features

FRONT PANEL FEATURES

1. ACCUMULATING DATA LED indicator. Illuminates in the accumulation mode (when taking measurements and accumulating the data). Indicates not only when transferring data, but when a measurement has been initiated and N measurements are not complete. Indicates when the 5358A has control over the 5345A.

2. OUTPUTTING DATA LED indicator. When illuminated and if addressed to talk, the 5358A is actually outputting data. When memory goes empty, it cannot output more data and the light goes out. Light blinks on and off as data is outputted, according to the output rate.

3. MEMORY FULL LED indicator. Indicates the 5358A memory circuits are full.

4. LISTEN LED indicator. When illuminated, indicates the 5358A has been addressed to listen on the bus.

5. TALK LED indicator. When illuminated, indicates the 5358A has been addressed to talk on the bus.

REAR PANEL FEATURES

6. ACCUM TRIG IN. BNC connector for external trigger input to System Control circuit. Provides for an external trigger to initiate data transfer as an alternate to the program code commands I (Initiate) or GET (Group Execute Trigger).

7. SAMPLE TIME MEAS OUT. BNC connector provides signal from Gate Control circuit for connection to 5345A GATE CONTROL INPUT. Controls the measurement period.

8. SAMPLE TIME DEAD OUT. BNC connector provides signal from Gate Control circuit for use with a *second* 5345A (GATE CONTROL INPUT). Controls the measurement period.

9. DEAD TIME START OUT. BNC connector provides for control of the start of dead (non-measurement) time by an external device.

10. DEAD TIME STOP IN. BNC connector provides for control of the stop of dead (nonmeasurement) time by an external device.

11. HP-IB connector. 24-pin connector used to interface the 5358A with the HP-IB. Conveys programming information to the 5358A and transfers data to and from the 5358A.

12. Control switch assembly. Switches A1 through A5 are address switches. The switch marked X is a FREE RUN switch, used to place the 5358A in the "TALK ALWAYS" mode. The switch marked Y sets the trigger level of the external trigger circuits to 1 or 4 volts.

13, 14. Umbilical connectors. Provide interconnection of power and control signals between 5345A and 5358A.

Figure 3-1. Front and Rear Panel Features (Continued)

3-10. PROGRAMMING

3-11. Bus Characteristics

3-12. The capability of a device connected to the HP-IB is specified by the interface functions that it has. *Table 3-1* lists the interface functions included in the 5358A. The "Interface Function Subset Identifier" refers to the particular capability of the interface function as listed in Appendix C of IEEE Standard 488-1975.

Table 3-1. HP-IB Interface Capability

INTERFACE FUNCTION SUBSET IDENTIFIER	INTERFACE FUNCTION DESCRIPTION
SH 1	Complete Source Handshake Capability
AH 1	Complete Acceptor Handshake Capability
T1	Talker (basic talker, serial poll, talk only mode, does not unaddress to talk if addressed to listen).
L2	Listener (basic listerner, no listen only mode, does not unaddress to listen if addressed to talk).
SR 1	Service Request Capability
RLØ	No Remote/Local Capability (remote only)
PPØ	No Parallel Poll Capability
DC1	Device Clear Capability
DT1	Device Trigger Capability
CØ	No Controller Capability
E1	1 Unit Bus Load

Interface functions provide the means for a device to receive, process, and send messages over the bus.

3-13. Bus messages are of 12 types. *Table 3-2* lists each bus message, a brief description of the message, and the response of the 5358A to the message. The last column shows typical examples of how to send/receive each message using the 9825A computing controller. For complete details on sending bus messages using the 9825A refer to the "9825A Extended I/O Programming Manual" (Part Number 9825-90025).

3-14. Address Selection

3-15. The 5358A must be assigned a bus address. *Table 3-3* gives the allowable address switch settings. Setting switches A2 through A5 defines four addresses: two listen and two talk addresses (switch A1 is not connected). The listen address labeled "program" (*Table 3-3*) is used to program the functions of the 5358A. The listen address labeled "data" is used to send data through the HP-IB to the 5358A. The two talk addresses defined by each switch setting function identically: either address allows the 5358A to output stored data or status byte information.

3-16. Before discussing the programming details of the 5358A, some discussion of 5345A programming is in order.

3-17. Programming the 5345A Electronic Counter

3-18. To use the full capability of the 5358A, certain guidelines must be followed when programming the 5345A. Several of the 5345A programmable functions interact with the programmable functions of the 5358A. For example, the 5345A must be programmed for EXTERNAL GATE if the 5358A is to provide the programmable gate signal to the 5345A. The following paragraphs discuss each group of 5345A codes and how they relate to programming the 5358A. *Table 3-4* contains the programming codes for the 5345A (Option 011) and is for reference.

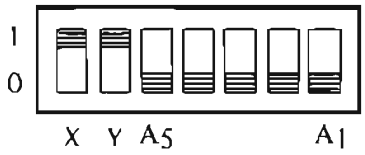
Table 3-2. 5358A Bus Message Usage

Message	Description	5358A Use	Sample 9825A Statement*
Data	Transfers device-dependent information from one device to one or more devices on the bus.	The 5358A listens at two addresses: one to receive programming codes, a second to receive data; both associated talk addresses output data or status byte information as appropriate.	(program listen) wrt 703, "R" (Data listen) wrt 702, "123" (Data talk) red 702, A
Trigger	Causes a group of slected devices to simultaneously initiate a set of device-dependent actions.	The 5358A begins to accumulate measurements	(Group Execute Trigger) trg 703
Clear	Causes an instrument to be set to a predefined state (a certain range, function, etc.).	The 5358A memory address register resets to zero	(Selected Device Clear) clr 703
Remote	Permits selected devices to be set to remote operation, allowing parameters and device characteristics to be controlled by Bus Messages.	NONE	rem 7 rem 711
Local	Causes selected devices to return to local (front panel) operation.	NONE	lcl 711
Local Lockout	Disables local (front panel) controls of selected devices.	NONE	llo 7
Clear Lockout and Local	Returns all devices to local (front panel) control and simultaneously clears the Local Lockout Message.	NONE	lcl 7
Require Service	Indicates a device's need for interaction with the controller.	Requests service depending on several condition (refer to paragraph 3-38)	if bit (7, rds (7)) = 1; gto ....
Status Byte	Presents status information of a particular device; one bit indicates whether or not the device currently requires service, the other 7 bits (optional) are used to indicate the type of service required.	Each status bit indicates a particular state of the 5358A (refer to para. 3-38).	Test the numerical value of a variable (e.g., A after executing rds (702)—A) for specific values
Status Bit	A single bit of device-dependent status information which may be logically combined with status bit information from other devices by the controller.	NONE	rqs 7,64
Pass Control	Passes bus controller responsibilities from the current controller to a device which can assume the Bus supervisory role.	NONE	pct 723
Abort	Unconditionally terminates Bus communications and returns control to the system controller.	5358A unlistens, untalks, and clears service request.	cli 7

*Assumes 5358A Address Switches $A_5A_4A_3A_2$=0001

Table 3-3. Addressing

ADDRESS SWITCH



HP-IB ADDRESS CODES

SWITCH SETTINGS				ASCII LISTEN ADDRESS		ASCII TALK ADDRESS		9825A DECIMAL ADDRESS
A_5	A_4	A_3	A_2	Code	Purpose	Code	Purpose	
0	0	0	0	SP !	Data Pgm	@ A	Data XX	0 1
0	0	0	1	" #	Data Pgm	B C	Data XX	2 3
0	0	1	0	$ %	Data Pgm	D E	Data XX	4 5
0	0	1	1	& '	Data Pgm	F G	Data XX	6 7
0	1	0	0	( )	Data Pgm	H I	Data XX	8 9
0	1	0	1	* +	Data Pgm	J K	Data XX	10 11
0	1	1	0	, -	Data Pgm	L M	Data XX	12 13
0	1	1	1	. /	Data Pgm	N O	Data XX	14 15
1	0	0	0	0 1	Data Pgm	P Q	Data XX	16 17
1	0	0	1	2 3	Data Pgm	R S	Data XX	18 19
1	0	1	0	4 5	Data Pgm	T U	Data XX	20 21
1	0	1	1	6 7	Data Pgm	V W	Data XX	22 23
1	1	0	0	8 9	Data Pgm	X Y	Data XX	24 25
1	1	0	1	: ;	Data Pgm	Z [	Data XX	26 27
1	1	1	0	< =	Data Pgm	\ ]	Data XX	28 29

XX = Not Used.
Pgm = Programming Code

NOTE

Address ASCII U,5 normally are reserved for the HP-IB controller.

Table 3–4. 5345A (Option 011) Programming Codes

1. FUNCTION — **ASCII**

a.	Plug In	F2
b.	Frequency A	FØ
c.	Period	F1
d.	Time Interval A to B	E3
e.	Ratio B/A	F5
f.	Start	F4
g.	Stop	F6

2. ACCUM MODE START/STOP (If F4 or F6)

a.	A+B	E=
b.	A–B	E5

3. REMOTE GATING

a.	External Gate	E;
b.	Internal Gate	E3

4. GATE TIME (If E3)

a.	10000 s	G4
b.	1000 s	G3
c.	100 s	G2
d.	10 s	G1
e.	1 s	GØ
f.	100 ms	G?
g.	10 ms	G>
h.	1 ms	G=
i.	100 µs	G<
j.	10 µs	G;
k.	1 µs	G:
l.	100 ns	G9
m.	Min	G5

5. INPUT AMPLIFIER CONTROL

a.	COM A or Separate	E7
b.	Check	E?

6. SAMPLE RATE SELECTION

a.	Maximum Sample Rate (~100 ms)	E1E4
b.	Minimum Time (≤100 µs)	E1E<
c.	HOLD	E9

7. OUTPUT MODE — **ASCII**

a.	ONLY IF addressed	E2
b.	WAIT until addressed	E:

8. DISPLAY POSITION

(Digits from E in Data String)
(Digit position defined from right to left, decimal point on right side of digit)

a.	Ø Digits	D;
b.	1 Digit	D:
c.	2 Digits	D9
d.	3 Digits	D8
e.	4 Digits	D?
f.	5 Digits	D>
g.	6 Digits	D=
h.	7 Digits	D<
i.	8 Digits	D3
j.	9 Digits	D2
k.	10 Digits	D1
l.	Auto Position + Auto Suffix Multiplier	DØ

9 DISPLAY MULTIPLIER SUFFIX (If other than DØ)

	FREQ	PERIOD TIME INTERVAL	START/ RATIO	
a.	GHz	ns	G	C7
b.	MHz	µs	M	C6
c.	kHz	ms	k	C5
d.	Hz	s		C4
e.	MHz	ks		C3

10. REMOTE PROGRAM INITIALIZE — I2

11. LOCAL — REMOTE

a.	Switch to Local	EØ
b.	Switch to Remote	E8

12. RESET — I1

13. SAMPLE TRIGGER COMMAND (If E9) — J1

RESET PUSHBUTTON/POWER UP/I2 PROGRAM conditions are FØ, GØ, DØ, E7, EØ, E2, E3, E1, E4, E5.

3-19. 5345A FUNCTION CODES. The 5345A functions that are programmable when used with the 5358A are:

FUNCTION	CODES
Frequency A	FØ
Period	F1
Time Interval A to B	F3
Ratio B/A	F5
Start	F4

3-20. 5345A REMOTE GATING AND GATE TIME CODES. If the 5358A is to provide the gate signal to the 5345A, then the 5345A must be programmed for External Gate (E;). When so programmed, the 5345A must also be programmed for Minimum Gate Time (G5). If decade gate times are desired, the 5345A may be programmed for Internal Gate (E3) and any of the Gate Time codes may be used.

3-21. 5345A SAMPLE RATE SELECTION CODES. These 5345A codes affect the dead time between measurements. If the 5345A is programmed for Minimum Time (E1E<) then the sample rate of the 5345A's output routine is completely bypassed. This implies that the programmed dead time will equal the actual dead time as long as the programmed number of digits can be transferred (a 5358A program code) during the dead time (see paragraph 3-31 for programming digits transferred and associated times). Do not use the 5345A HOLD command (E9).

3-22. MISCELLANEOUS 5345A CODES. The output mode on the 5345A must be ONLY IF Addressed (E2). The Remote Program Initialize (I2) and Reset (I1) codes function normally. The 5345A must be programmed for Remote (E8) in order to function with the 5358A. Whenever a Reset (I1) command is sent to the 5345A, at least 50 ms is required for the counter to initialize.

3-23. Programming the 5358A

3-24. *Table* 3-5 gives the Program Code Set for the 5358A. The codes are functionally grouped and, in general, one code should be selected from each group. Codes should be selected for use in a program code string in the same order that the groups are listed. Detailed explanation of each group follows.

3-25. COUNTER HOLD-OFF. The 5358A is capable of arresting the measurement cycle of the 5345A and holding the counter in a prearmed state. When the counter hold-off is enabled (5358A programmed with ASCII G3) there is no gate signal (SAMPLE TIME MEAS OUT) applied to the 5345A and the 5345A is prevented from arming. If disabled (5358A programmed with G2), a gate signal is applied to the counter and the counter is able to make measurements. In either case, sending an ASCII "I" to the 5358A allows the storage of measurements (paragraph 3-34).

3-26. ACCUMULATE MODE. The 5358A can be programmed to make either a specified number of measurements (counted mode) or to make measurements continually (not counted mode). If programmed in the counted mode (G1), then (1) the number of measurements are programmed by using the N code (paragraph 3-30) and (2) the service request message is sent when the measurements are complete (paragraph 3-36). In either mode, there are three ways to initiate measurements: (1) send the trigger message, (2) send an accumulate initiate commade (I) or, (3) externally trigger the 5358A. In either mode, if the memory fills up, the accumulation of measurements will stop and the 5358A will send the service request message. When the memory is full, reading data from the 5358A will cause additional measurements to be made until the programmed number are made (if counted mode) or on accumulate halt command (H) is issued to the 5358A. To halt the accumulation of measurements in a synchronized manner (no data lost), program the 5358A for counted mode (G1) and counter hold-off enabled (G3).

Table 3-5. 5358A Program Code Set

FUNCTION	ASCII CODE
Counter Hold-Off	
Disabled	G2
Enabled	G3
Accumulate Mode	
Counted	G1
Continuous	G0
External Trigger	
Disabled	G4
Enabled	G5
Slope -	G6
Slope +	G7
Dead Time (must be programmed prior to measurement time)	
Minimum	D0K
Ratio (Meas/Dead) 1:1	D1K
Ratio (Meas/Dead) 2:1	D2K
External	
Start Slope + , Stop Slope +	D3K
Start Slope + , Stop Slope -	D7K
Start Slope - , Stop Slope +	D;K
Start Slope - , Stop Slope -	D?K
Measurement Time Prefix	M
Range (μs)	1E0 to 999E7
Suffix	K
Number of Measurement Stored Prefix	N
Range	1 to 9999
Number of Digits Transferred from 5345A Prefix	T6
Range	1 to 13
Output Format - Packed BCD (Reversed)	F0
ASCII (<time>, <events> CR LF)	F1
Packed BCD (nonreversed)	F2
Memory Reset (to Empty) Command	R (or clear)
Accumulate Initiate Command	I (or trigger)
Accumulate Halt Command	H

3-27. EXTERNAL TRIGGER. The 5358A may be triggered (start measurement accumulation) externally by supplying a start pulse to the ACCUM TRIG IN rear panel BNC connector. The Y switch on the rear panel address switch bank selects either a 1-volt (50Ω load) or 4-volt (TTL load) trigger level; the Ø-position selects the 4-volt level while the 1-position selects the 1-volt level. To enable external triggering, program the 5358A with ASCII G5. In addition, the slope of the trigger signal can be selected by programming the 5358A with G6 (- slope) or G7 (+ slope). To disable the external trigger function, program an ASCII G4.

3-27. DEAD TIME. Dead time is the time during which a measurement not being taken. The dead time is used by the 5358A to transfer the previously completed measurement from the 5345A internal data bus to the 5358A memory. The amount of time used by the 5345A to transfer digits depends on how many digits are transferred. The required transfer time is given by:

$$Y = 7 + 2X$$

Where: Y = total transfer time in microseconds
X = programmed number of digits transferred (paragraph 3-31).

The minimum dead time (DØK) is that time specified by the above equation. The dead time may also be specified to be equal to the measurement time (D1K) or twice the measurement time (D2K). Note that it is possible to program a dead time less than the required amount of time needed for measurement transfer. If this occurs in operation, the 5358A will service request, and set bit 2 of the status byte low (paragraph 3-36). The dead time stop signal may be supplied externally by applying pulses to the rear panel input connector labeled DEAD TIME STOP IN. This signal is triggered, with a programmed delay, by the signal from the rear panel output connector labeled DEAD TIME STOP OUTPUT. The trigger slopes are programmable by the following program codes:

START SLOPE	STOP SLOPE	5358A PROGRAM CODE
⌐¯	⌐¯	D3K
⌐¯	¯⌙	D7K
¯⌙	⌐¯	D;K
¯⌙	¯⌙	D?K

If the dead time that results from the externally supplied signal is less than the time required to transfer digits, then the 5358A will service request and set bit two the status byte low (paragraph 3-36).

3-29. MEASUREMENT TIME. The measurement time is the time during which the 5345A is counting the zero crossings of the input signal. The measurement time is specified in units of microseconds from 1EØ to 999E7 microseconds. To program the measurement time send M followed by the time in microseconds followed by K. For example, to program a measurement time of 1.2 seconds, send either M12E5K or M120E4K.

3-30. NUMBER OF MEASUREMENTS TO BE STORED. The 5358A can be programmed to make a specified number of measurements. The 5358A must first be programmed in the counted accumulate mode (G1, paragraph 3-26). To program the number of measurements, send N followed by from 1 to 4 digits in the range 1 to 9999. The specified number of measurements may be larger than the memory size of the 5358A. Depending on the number of digits transferred (paragraph 3-31), the 5358A memory may fill up prior to completion of the requested number of measurements. For example, let the number of digits transferred (T) be set to 1. By definition, one measurement is made up of an events count and a time count received from the 5345A in BCD format. One measurement, then, can be stored in one byte of 5358A memory (T=1): the single digit (BCD) representing the events count in bits 0 through 4 and the single digit (BCD) representing the time count in bits 5 through 8. Thus with one measurement per byte (T=1), 2048 measurements can be acquired before memory is filled (MEMORY FULL indicator lites after the 2048th measurement is stored). For more information

on memory storage format refer to paragraph 3-32. In this example, if 4000 measurements are specified, the first 2048 will be acquired using the programmed dead time. The dead time for the last 1952 measurements will depend on how fast the calculation can make room in the memory by reading out previously made measurements: as each measurement is read out of the 5358A, a new measurement is automatically made and stored in the vacant memory location(s).

3-31. NUMBER OF DIGITS TRANSFERRED. The 5358A can be programmed to transfer from 1 to 13 digits (BCD) from the 5345A into memory. The specified measurement time determines how many digits are significant. For example, a 1-second measurement time will produce approximately nine significant digits for the time count in the 5345A (clock period = 2 ns). A measurement time of 1-microsecond creates three significant digits. *Figure 3-2* shows the number of significant digits versus measurement (gate) time. The 5358A should be programmed to transfer at least as many digits as indicated in *Figure 3-7*. To program the 5358A for number-of-digits-transferred send ASCII T followed by 1 or 2 ASCII digits in the range of 1 to 13. The number of digits specified affects how many measurements can be stored in the 5358A before the memory becomes full (see paragraph 3-32).

3-32. OUTPUT FORMAT. There are three programmable modes for the output format. Before discussing the output formats the 5358A data storage map will be described. The 5345A counts time and events for the specified measurement period (gate signal). The 5358A is programmed to transfer, for example, T digits of both the events and the time count into memory. An example demonstrates how the data is stored.

For: T=3 (3 digits transferred)
1 μs gate
Input to 5345A = 25 MHz

The: Time count = 500
Events count = 025

The data is stored in the 5358A memory as follows (numbers are BCD digits).

	Upper 4 bits	Lower 4 bits	
Byte 1	2	5	events
Byte 2	0	0	
Byte 3	5	0	time

As can be seen, the events are stored first, least significant digit (LSD) first. The time is stored next, also LSD first. Note that the data is packed, i.e., there are no "wasted" bits. In general, the storage map for a transfer of T digits looks like:

	T odd			T even	
Byte 1	E_2	E_1	Byte 1	E_2	E_1
Byte 2		E_3	Byte 2		E_3
Byte (T+1)/2	τ_1	E_T τ_2	Byte T/2	E_T τ_2	E_{T-1} τ_1
Byte T	τ_T	τ_{T-1}	Byte T	τ_T	τ_{T-1}

Where: Events count = E_T E_{T-2}
Time count = τ_T τ_{T-1} ... τ_2 τ_1
(each digit is BCD)

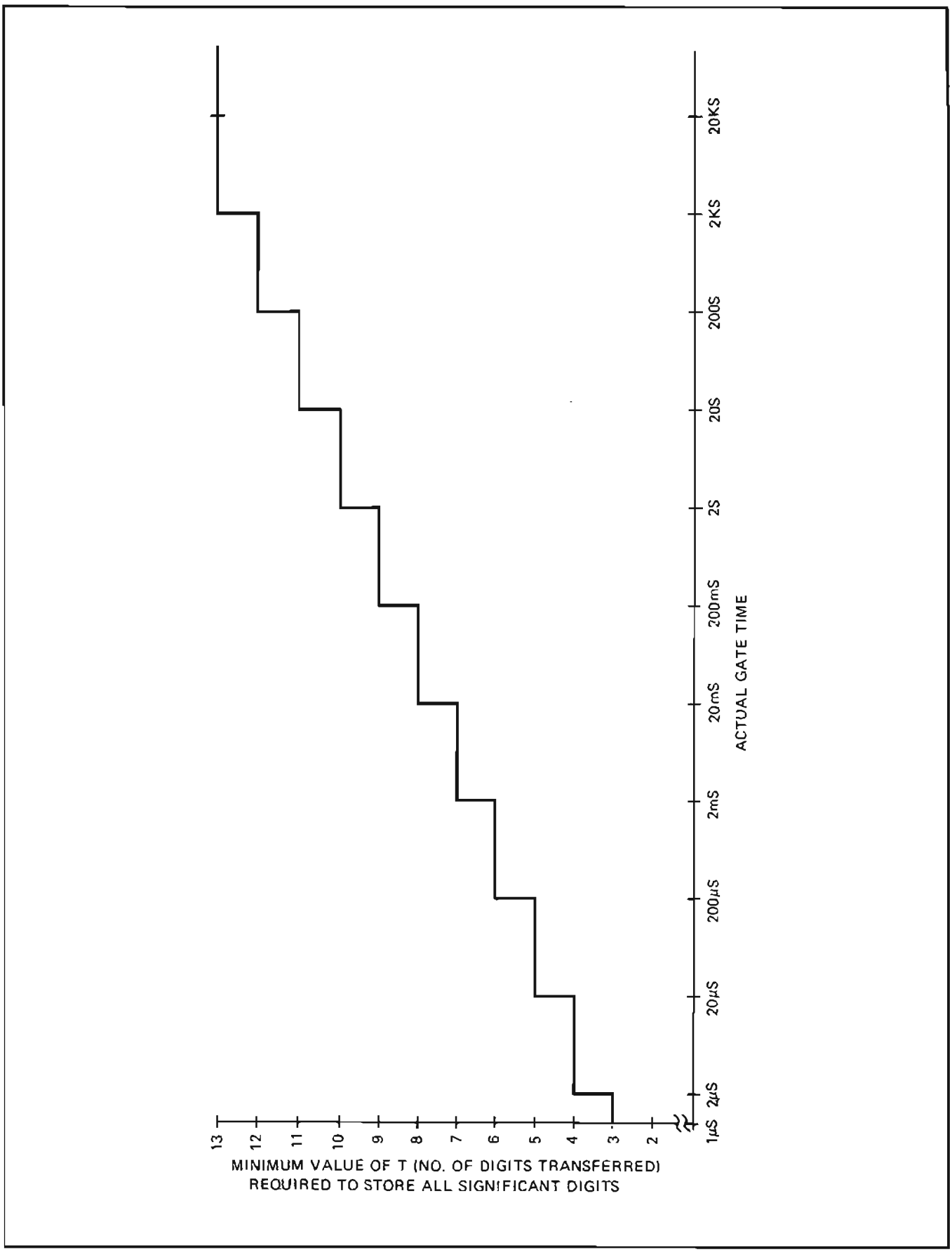


Figure 3-2. Significant Digits versus Measurement Time

The data storage map is independent of the specified output format. The output formats are:

Name	ASCII Program Code
Packed BCD-reversed	FØ
ASCII	F1
Packed BCD-nonreversed	F2

It is easiest to explain the packed BCD-nonreversed (F2) first. Using the above symbology, the sequence of bytes output to the HP-IB are (T odd):

	Upper 4 bits	Lower 4 bits
Byte 1	E_2	E_1
Byte 2		E_3
Byte (T+1)/2	τ_1	E_T
Byte T	τ_T	τ_{T-1}

The packed BCD-reversed (FØ) is very similar except the order of the bytes is reversed:

	Upper 4 bits	Lower 4 bits
Byte 1	τ_T	τ_{T-1}
Byte (T+1)/2	τ_1	E_T
Byte T-1		E_3
Byte T	E_2	E_1

The ASCII output format (E_1) is the easiest to use. For a transfer to T digits the order of output is:

Byte 1	τ_T
Byte 2	τ_{T-1}
Byte T	τ_1'
Byte T+1	,
Byte T+2	E_T
Byte T+3	E_{T-1}
Byte 2T+1	E_1'
Byte 2T+2	CR
Byte 2T+3	LF

The primed quantities are the ASCII code for the stored BCD digits. The ASCII format (F1) is the standard output format for most HP-IB instruments. To program the output format send FØ or F1 or F2 to the 5358A.

3-33. MEMORY RESET. There are two ways to reset the 5358A memory: send ASCII R or send the clear bus message (selected device clear or device clear). The response of the 5358A to the reset commands is to empty memory (memory address counter set to zero).

3-34. ACCUMULATE INITIATE. There are two ways to program the start of measurement storage: send ASCII I or send the trigger message (group execute trigger). Refer to paragraphs 3-25 and 3-26 for additional discussion.

3-35. ACCUMULATE HALT. To program the halt of measurement accumulation (assuming it is desirable to stop making measurements before the programmed numbers are completed if G1 or to stop the continuous accumulation if GØ, paragraph 3-26), send ASCII H to the 5358A. When halted, the counter continues to make measurements but they are not stored if G2 or the counter's arming is inhibited if G3 (paragraph 3-25).

3-36. Status Byte Description

3-37. The 5358A is designed to send the status byte message. When serial polled, the 5358A outputs an 8-bit byte (STB1 through STB8). The active (1) state of each bit indicates the status as follows:

STB1 Power down at some previous time. (A second request is necessary to determine if the power down is a present (current) condition.)

STB2 Real Dead Time > Programmed Dead Time

STB3 Counter in "HOLD" until memory is not full

STB4
STB5 Memory Status

STB5	STB4	
0	0	Empty
0	1	<1/2 Full
1	0	≥1/2 Full
1	1	Full

STB6 Counted measurements complete

STB7 Service request (actived by one of the following conditions):

- Power up/down condition
- Real dead time > programmed dead time
- Counted measurements completed
- Memory full

STB8 Not assigned

3-38. Description of Status Byte Bits

STB1 Power Down. If B1 is active, a power failure in the 5358A is indicated. This status bit is a latched bit so the indication could be caused by a past failure or a present failure. After status is read out the 5358A status circuit is cleared so a second request from the calculator is required to determine if the condition is a current one.

STB2 Read Dead Time > Programmed Dead Time. If B2 is active it indicates that the read dead time exceeds the programmed dead time. The dead time is determined by programming the measurement time and programming the ratio of measurement time to dead time (minimum, 1:1, 2:1, External) in terms of microseconds. An error in programming could result in this status indication. For example, if the measurement time programmed is far below the capability of the 5345A to transfer data and get back into the measurement mode. Also, if the SAMPLE RATE control of the 5345A is active, it will result in additional time between the processing cycle and the measurement cycle which will add to the real dead time and cause it to exceed the programmed dead time. When

programming, the 5345A SAMPLE RATE should be disabled via the HP-IB to prevent this excessive dead time (paragraph 3–21). This status condition does not occur if the 5358A dead time is programmed to minimum. Another cause of excessive read dead time could be the result of the 5358A memory becoming full.

STB3 Counter in "HOLD" until memory is not full. An active STB3 indicates that the 5345A is being "held" between the measurement cycle and the processing cycle. This condition occurs when the 5358A memory becomes full. If STB2 is active and STB3 is active the indication is that the real dead time is excessive due to the memory full condition.

STB4, STB5 Memory Status. The state of B4 and B5 indicates the status of the 5358A memory, as follows:

STB5	STB4	
0	0	Empty
0	1	<1/2 Full
1	0	≥1/2 Full
1	1	Full

For example, if STB4 and STB5 are both in the "1" state, memory is full. As stated in the STB3 description above, an active STB2 would indicate that the memory full condition is causing excessive real dead time.

STB6 Counted Measurements Complete. An active STB6 indicates that the programmed number of measurements (N) has been completed.

STB7 Service Request. When STB7 is active the 5358A is in a service request condition and the Service Request (SRQ) signal is sent via the HP-IB SRQ line to the calculator. Any of the following status conditions will activate the service request:.

STB1 — Power up/down condition
STB2 — Read dead time > programmed dead time
STB6 — Counted measurements complete
STB4 and STB5 — Memory full

3–39. Latched Status Bits

3–40. Status bits STB1, STB2, STB3, and STB6 are latched bits, which means that their status remains active (latched) until a status request from the calculator causes a readout and clears the latched condition. This means that an active condition of any of these bits could be a current condition or could be a past condition that was not previously readout. The way to determine if the condition is current is to send a second status request which will readout the current status.

3–41. Default Conditions

3–42. On power up, the G register will automatically be programmed to the GØ, G2, G4, and G6. The T-register comes up as a 14 (T14). The F-register comes up as 1 (F1). The D-register comes up as DØ. The E-register comes up as Ø. Main memory comes up as Empty, as does all status byte bits except bits 1 and 7. The N-register and the matissa register do not power up in any prestate. The power-up service request status bit 1 comes up active.

3–43. Programming Examples

3–44. The following 9825A sample program is provided for information only. Other programming examples may be found in Section IV, Performance Tests. The example in paragraph 4–15

programs the 5358A for external trigger. The example in paragraph 4–17 programs the 5358A for external dead time and the example in paragraph 4–19 programs the 5358A for a gate signal of 5 ms. The program shown here was written for a 5345A with address switches A_5 A_4 A_3 A_2 set to 0101 (A_1 does not care) and 5358A address switches A_5 A_4 A_3 A_2 set to 0110 (A_1 does not care). The sample at the left by line number:

```
0: dim A$[10,15]
1: wrt 710,"I2F0
 E;G5E?E1E<E2E8I
 1"
2: wait 50
3: wrt 713,"G2I4
 D0KM1E3N10T6F1R
 I"
4: rds(713)→S
5: if bit(5,S)=1
 ;sto 7
6: sto 4
7: 0→I
8: rds(713)→S
9: if bit(3,S)=0
  and bit(4,S)=0
 ;sto 14
10: I+I→I
11: red 713;A$[I
 ]
12: prt A$[I]
13: sto 8
14: fxd 0;prt
 "No of meas.
 =";I
15: stp
*15179
```

Line	Purpose
0:	Dimension string variable A$
1:	Program the 5345A for: I2 Remote Program Initialize FØ Frequency A E; External Gate G5 Minimum Gate Time E? Check E1E< Minimum Sample Rate E2 Output Only if Addressed E8 Go to Remote I1 Reset
2:	Wait 50 ms after sending Reset to 5345A
3:	Program the 5358A for: G2 Counter Hold-Off Disabled G1 Counted Mode G4 External Trigger Disabled DØK Minimum Dead Time M1E3 1 ms Gate Time N10 Acquire 10 measurements T6 Transfer 6 digits F1 ASCII Output Format R Reset I Initiate
4:	Read 5358A Status
5:	Check status byte bit 5 for true (SRQ true). Note: 9825A labels byte bits 0 through 7 whereas 5358A labels these bits 1 through 8.
6:	Loop if SRQ not true
7:	Counter for number of measurements
8:	Read 5358A Status
9:	Check 5358A status byte bits 4 and 5 for memory empty; stop if empty.
10:	Increment Count I
11:	Read measurement into A$
12:	Print A$
13:	Loop if not empty
14:	Print number of measurement made
15:	Stop

Note that the first reading is significantly different from the remaining reading due to the non-synchronization between the 5345A measurement cycle and the 5358A Initiate measurement command. However, the division of the events count by the time count (multipled by 500 MHz to obtain frequency) is constant for all readings.

SECTION IV
PERFORMANCE TESTS

4–1. INTRODUCTION

4–2. This section provides an In-Cabinet Performance Test for the 5358A installed in the 5345A (refer to *Figure 4–1* for interconnections), connected to a 9825A Controller and a 9871A or 9866B Printer. The performance test consists of two main tests. The first test is the Diagnostic Program and the second test exercises the rear panel I/O jacks (BNC) connections).

WARNING

ANY ADJUSTMENT, MAINTENANCE, AND REPAIR OF THE OPENED INSTRUMENT UNDER VOLTAGE SHOULD BE AVOIDED AS MUCH AS POSSIBLE AND, WHEN INEVITABLE, SHOULD BE CARRIED OUT ONLY BY A SKILLED PERSON WHO IS AWARE OF THE HAZARD INVOLVED.

4–3. TEST EQUIPMENT

4–4. *Table 1–3* lists test equipment recommended for maintaining and checking the performance of the 5358A Measurement Storage Plug-In. Test equipment with equivalent characteristics may be substituted.

4–5. IN-CABINET PERFORMANCE CHECKS

4–6. The performance checks are used to verify and record proper operation of the circuits in the 5358A plug-in. It may serve as:

a. Part of an incoming inspection check of plug-in specifications.
b. A periodic check.
c. Part of a procedure to locate defective circuits.
d. A permanent record of instrument maintenance.

4–7. There are two types of tests. The first test is a fully automatic test performed by the controller. The software for the test is on a tape cartridge (HP Part Number 05358–16000). This automatic test checks all the major functions of the 5358A. The second test checks the operation of the rear panel I/O (BNC connections). This is performed by the controller along with an added Pulse Generator (see *Figure 4–3*). The software for the second test is supplied in paragraphs 4–16 through 4–19. For a listing of the diagnostic program, refer to paragraph 4–22 at the end of this section.

4–8. Diagnostic Operating Procedure

4–9. The diagnostic program is provided on a tape cartridge for the 9825A Controller with 9871A or 9866B Printer. For the diagnostic program to work properly, the equipment must be properly connected and all address switch settings must be correctly set. Refer to *Figure 4–1* for proper set-up.

4–10. To run the 5358A diagnostic, proceed as follows:

a. Apply power to equipment.
b. Insert software cartridge (P/N 05358–16000) into 9825A Controller.
c. Install special functions key overlay, shown in *Figure 4–2*, labeled DIAGNOSTIC CONTROL.

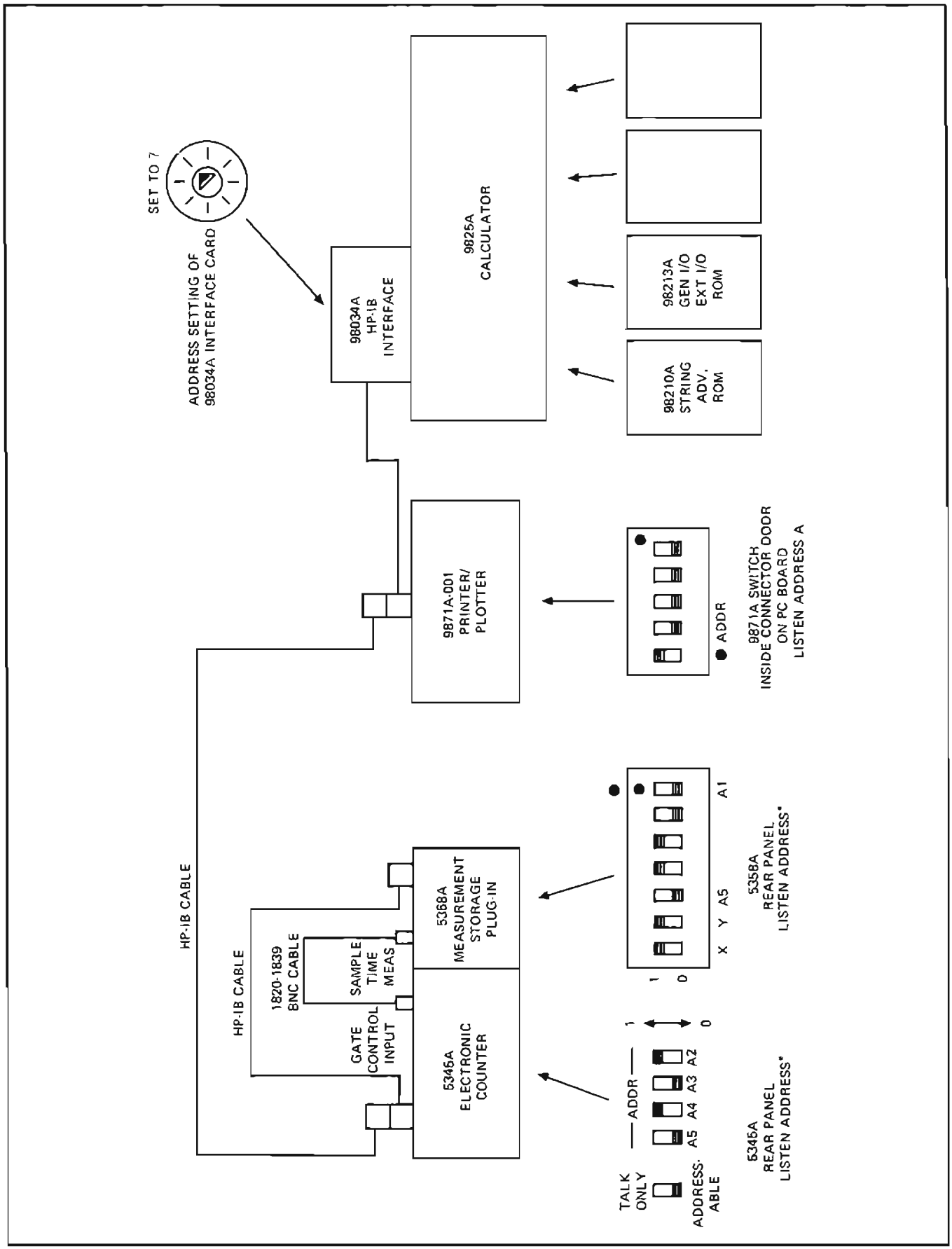


Figure 4–1. Diagnostic Test Interconnections

d. Load the program by setting the calculator power switch to OFF position, then back to ON position or by typing ldp1 EXECUTE.

e. Monitor the 9825A display for "enter program name," then press keys as listed below:

NOTE

To obtain a calculator printer listing of programs available, type HELP and press CONTINUE key.

NOTE

The ID# listed below is as set at the factory. If these values have been changed, use the current values.

Press 9825A Key — **9825A Display**

enter program name

5 3 5 8 A

NOTE

If program name is not correctly entered, the statement, "program not found" or "program not available yet" will be displayed.

[CONTINUE]

ENTER PRINT DEV ID#

If printer is a 9871A, type 701 and press [CONTINUE] key. If printer is a 9866B, type 6 and press [CONTINUE] key.

ENTER 5358A DEV ID#

Type 712 and press [CONTINUE]

ENTER 5345A DEV ID#

Type 710 and press [CONTINUE]

ENTER MEM SIZE

Type 2 (if 2K 5358A)
Type 4 (if 4K 5358A)
Type 6 (if 6K 5358A)
Type 8 (if 8K 5358A)
and press [CONTINUE]

SELECT KEY FUNCTION

Press Special Function Key f_5 for RUN ALL TEST

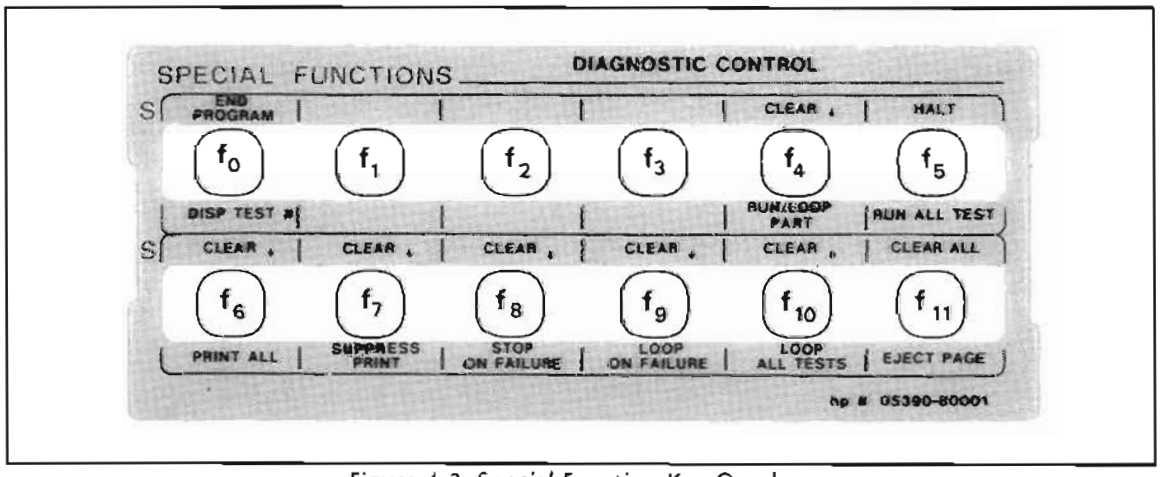


Figure 4-2. Special Function Key Overlay

4-11. For an explanation of Diagnostic errors and troubleshooting, refer to Section VIII.

4–12. Rear Panel I/O Performance Test Procedure

4–13. There are five input/output BNC connectors on the rear panel of the 5358A. The MEAS SAMPLE TIME was checked during the diagnostic program. Paragraphs 4–14 and 4–20 give the procedures for checking the remaining four BNC inputs and outputs.

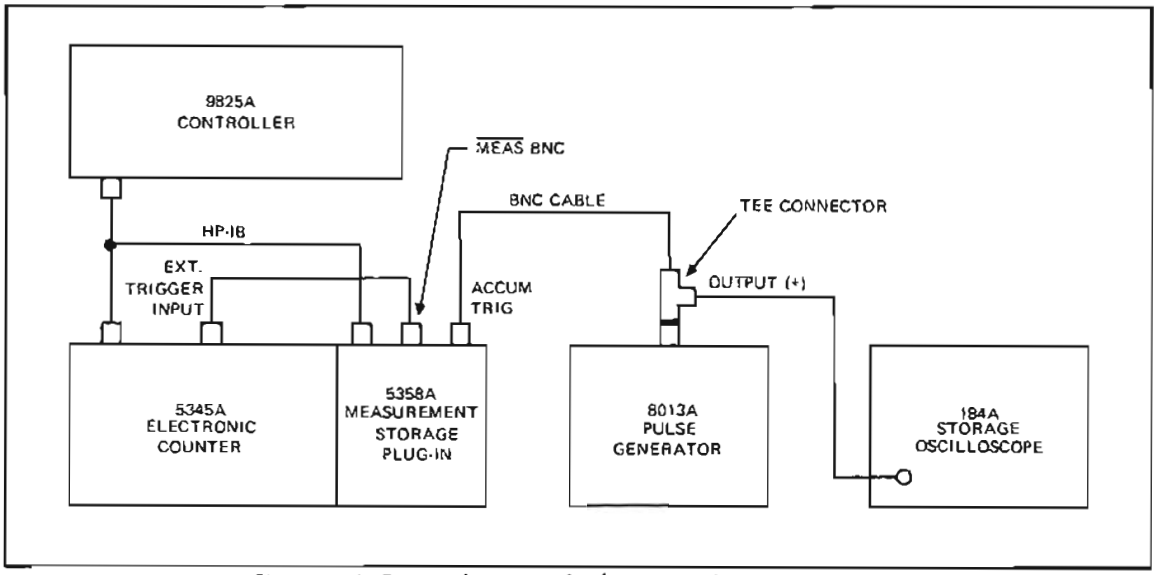


Figure 4–3. External Trigger Performance Interconnection

4–14. External Trigger

4–15. Refer to *Figure 4–3* and proceed as follows:

1. Connect the 5358A ACCUM TRIG BNC input to the output of the 8013A Pulse Generator with a BNC cable and a tee connector.
2. Connect the input (1 megohm) of the 184A oscilloscope to the tee connector.
3. Set the "Y" switch (switch in the 5358A rear panel address switch array) in the down (Ø) position (TTL input).
4. Adjust the 8013A output for a pulse width of 100 ns with a pulse period of 2 μs. The dc offset of this signal must be +0.8V from ground reference and +2.4V in amplitude from ground reference as shown in *Figure 4–4A*. Set the pulse delay to 35 ns with the vernier in maximum ccw.

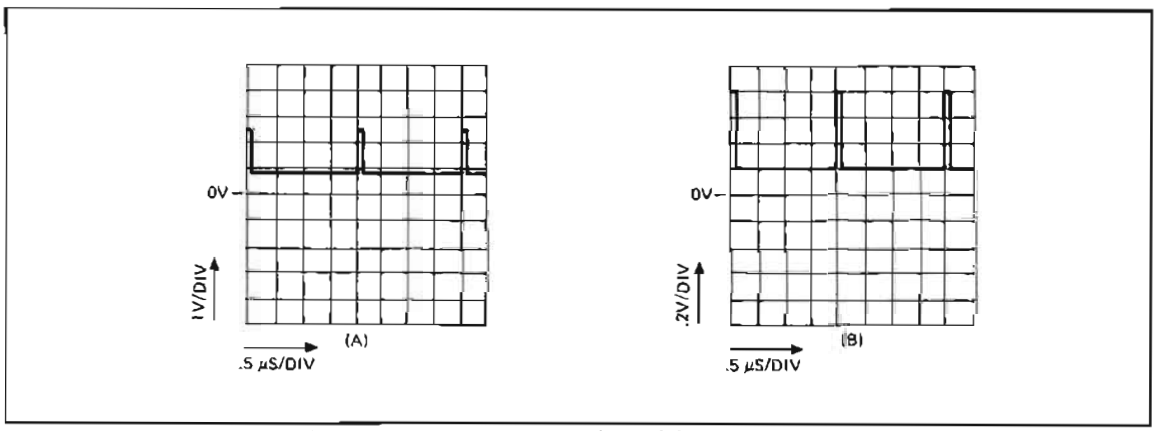


Figure 4–4. 8013A Output for ACCUM TRIG Test

5. Key the program shown in *Figure 4-5* into the 9825A.

```
0: wrt 710,"I2G5
 E;?<8I1"
1: wrt 713,"G134
 N9999T1D0KM1E3K
 RH"
2: dsp "PRESS CO
 NTI&WATCH FOR
 MEM FULL"
3: stp
4: wrt 713,"G5".
*15513
```

Figure 4-5. ACCUM TRIG Program

6. With the program in *Figure 4-5* loaded, press the RUN key of the 9825A. When the message is displayed, press the CONTINUE key and watch for the MEMORY FULL light on the 5358A front panel. This should take about 2 seconds for every 2K of memory in the 5358A. The ACCUMULATING DATA light will also be on until memory goes full. The memory full condition indicates the external trigger operates in "Y" 0 (TTL load, 4-volt) position.
7. Set the "Y" switch in the 1 (50 ohm load, 1-volt) position and adjust the 8013A output for a dc offset level of +0.2V from ground reference and +0.8V in amplitude from ground reference as shown in *Figure 4-4B*.
8. Again, press the RUN key on the 9825A and then the CONTINUE key watching for the MEMORY FULL light on the 5358A front panel. The memory full condition indicates the external trigger operates in the "Y" up (50 ohm load) position.

4-16. Dead Time — Start, Stop

4-17. Refer to *Figure 4-6* and proceed as follows.

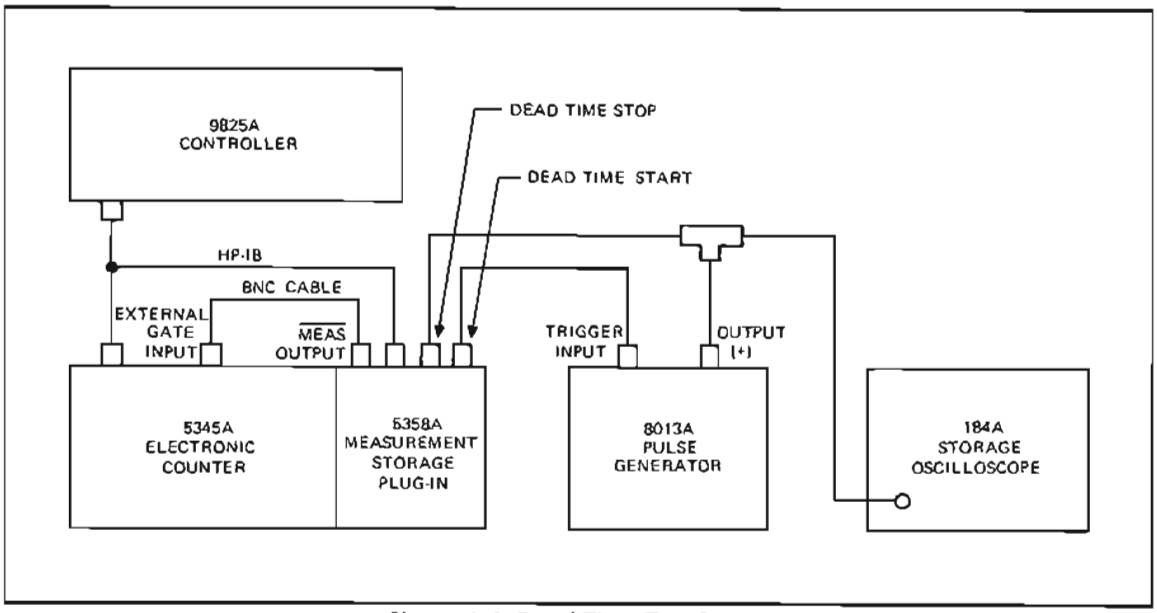


Figure 4-6. Dead Time Test Setup

1. Connect the 8013A trigger input and (+) output to the 5358A DEAD TIME START and DEAD TIME STOP with a tee connector on the (+) output of the 8013A. Run a BNC cable from the tee to the 184A oscilloscope.
2. Readjust the 8013A for a 100 ns pulse +0.8V offset from ground and +2.4V in amplitude from ground (*Figure 4-4A*) reference.
3. Set the PULSE PERIOD switch to the (+) EXT position. The signal should disappear from the oscilloscope screen.
4. Key the program shown in *Figure 4-7* into the 9825A.

```
0: wrt 710,"I2G5
 E;K?8I1"
1: wrt 713,"G31N
 9999T1D0Km1E3KR
 H"
2: dsp "PRESS[CO
 NT]&WATCH FOR
 MEM FULL";stp
3: wrt 713,"D3K"
 ,"I"
*15413
```

Figure 4-7. External Dead Time Program

5. Press the RUN key of the 9825A. When the message is displayed, press the CONTINUE key and watch for the MEMORY FULL light on the 5358A front panel. This should take about 2 seconds for every 2K of memory in the 5358A.

4-18. DEAD Rear Panel BNC Connector

4-19. Key the program shown in *Figure 4-8* into the 9825A. Then press the RUN key on the 9825A.

```
0: wrt 710,"I2G5
 E7;8I1"
1: wrt 713,"G204
 T8D1KF1M5E3KRI"
2: red 712,A
3: eno 2
*716
```

Figure 4-8. DEAD BNC Output Program

4-20. Connect the 184A scope probe to the DEAD BNC on the rear panel of the 5358A. Adjust the 184A horizontal sweep to 2 ms/div. Approximately 2 complete cycles should be displayed with an amplitude of about -5V.

4-21. Successful completion of the performance tests verifies the proper operation of the circuits in the 5358A plug-in.

4–22. *Figure 4–9* shows a functional block diagram of the 5358A diagnostic program. File 1 contains the SPECIAL FUNCTION KEY definitions. File 2 contains the diagnostic resident segment which, when driven by the special function keys, loads the appropriate file containing the actual diagnostic test section (note, all files are on track one). In order to obtain a listing of the program, the diagnostic program must be loaded, as if to test the 5358A, and started running. Then the diagnostic can be stopped and a listing made. The following procedure will produce the 5358A diagnostic program listing;

STEP 1 Execute the usual procedure for starting the 5358A diagnostic responding to the 9825A messages in the normal fashion (see Section IV) until the 9825A display returns with (SELECT KEY FUNCTION).

STEP 2 Press f_4. Respond to "ENTER <sec #> .<test #> | , <sec #> " by typing 1 CONTINUE. Press STOP. Type list #701 EXECUTE. The 9871A then lists the resident segment (lines 0 through 149) and the section of the diagnostic (lines 150 through 235) stored on file 3.

STEP 3 Press f_4 when the listing is complete. Respond to "ENTER <sec #>..." by typing 7 CONTINUE. Press STOP. Type list #701, 150 EXECUTE. The listing obtained (lines 150 through 242) contains the sections of the diagnostic stored on file 4.

STEP 4 Repeat step 3 except respond to "ENTER..." by typing 1 3 CONTINUE. Press STOP. Type list #701, 150 EXECUTE. The listing obtained (lines 150 through 231) contains that portion of the diagnostic stored on file 5.

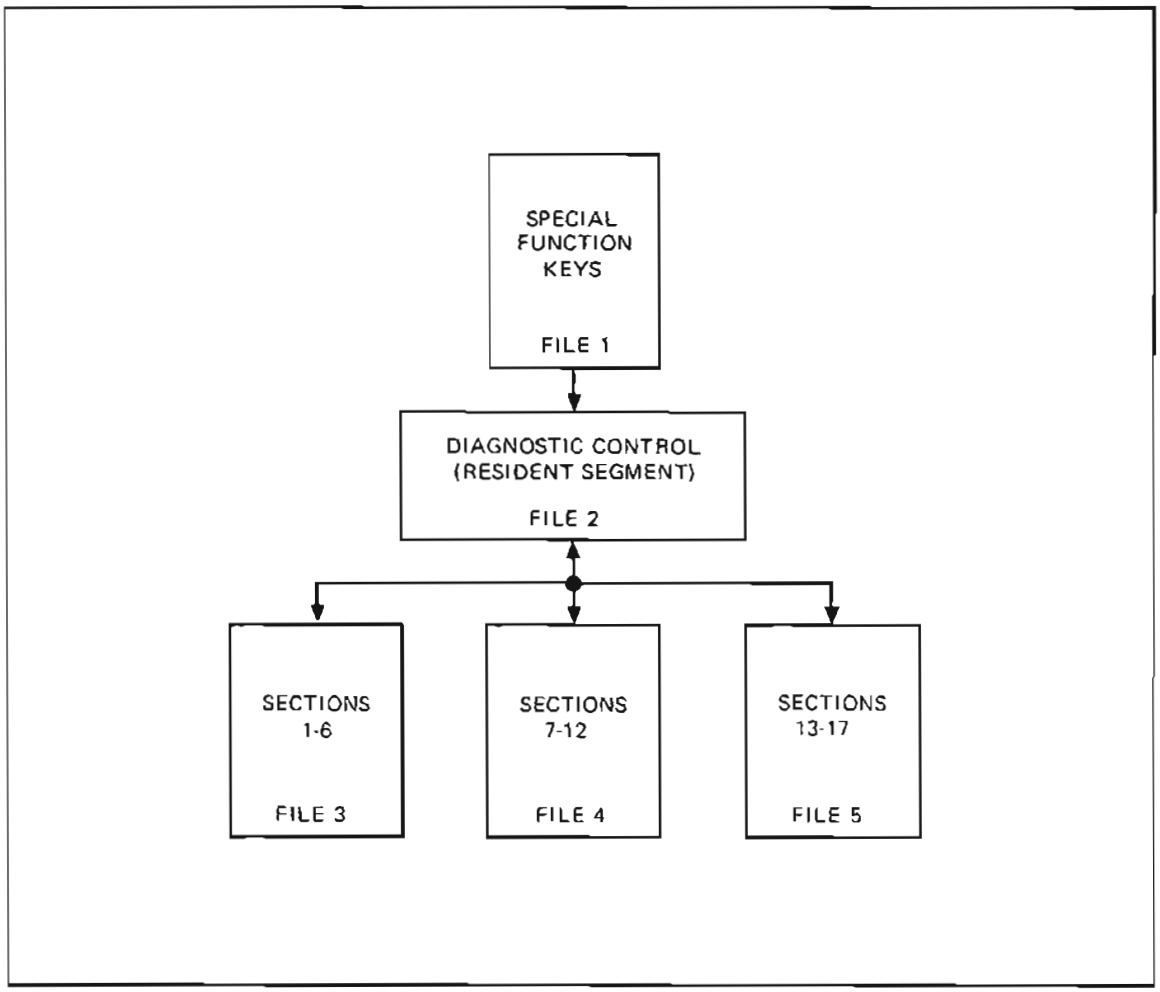


Figure 4–9. Functional Block Diagram of the 5358A Diagnostic Program

SECTION V
ADJUSTMENTS

5–1. GENERAL

5–2. The 5358A circuits do not require any adjustments.

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering replacement parts. Table 6-1 lists parts in alphanumerical order of their reference designators and indicates the description and HP Part Number of each part, together with any applicable notes. The table includes the following information:

a. Description of part (see abbreviations below).

b. Typical manufacturer of the part in a five-digit code; see list of manufacturers in Table 6-2.

c. Manufacturer's part number.

d. Total quantity used in the instrument (Qty column).

REFERENCE DESIGNATIONS

A	= assembly	E	= miscellaneous electrical part	MP	= miscellaneous mechanical part	TP	= test point
AT	= attenuator, isolator, termination	F	= fuse	P	= electrical connector (movable portion); plug	U	= integrated circuit; microcircuit
B	= fan, motor	FL	= filter			V	= electron tube
BT	= battery	H	= hardware	Q	= transistor; SCR; triode thyristor	VR	= voltage regulator; breakdown diode
C	= capacitor	HY	= circulator	R	= resistor	W	= cable; transmission path; wire
CP	= coupler	J	= electrical connector (stationary portion); jack	RT	= thermistor	X	= socket
CR	= diode; diode thyristor; varactor	K	= relay	S	= switch	Y	= crystal unit–piezoelectric
DC	= directional coupler	L	= coil; inductor	T	= transformer	Z	= tuned cavity, tuned circuit
DL	= delay line	M	= meter	TB	= terminal board		
DS	= annunciator, signaling device (audible or visual); lamp; LED			TC	= thermocouple		

ABBREVIATIONS

A	= ampere	BCD	= binary coded decimal	COMP	= composition	°K	= degree Kelvin
ac	= alternating current	BD	= board	COMPL	= complete	DEPC	= deposited carbon
ACCESS	= accessory	BE CU	= beryllium copper	CONN	= connector	DET	= detector
ADJ	= adjustment	BFO	= beat frequency oscillator	CP	= cadmium plate	diam	= diameter
A/D	= analog-to-digital	BH	= binder head	CRT	= cathode-ray tube	DIA	= diameter (used in parts list)
AF	= audio frequency	BKDN	= breakdown	CTL	= complementary transistor logic	DIFF AMPL	= differential amplifier
AFC	= automatic frequency control	BP	= bandpass	CW	= continuous wave	div	= division
AGC	= automatic gain control	BPF	= bandpass filter	cw	= clockwise	DPDT	= double-pole, double-throw
AL	= aluminum	BRS	= brass	D/A	= digital-to-analog	DR	= drive
ALC	= automatic level control	BWO	= backward-wave oscillator	dB	= decibel	DSB	= double sideband
AM	= amplitude modulation	CAL	= calibrate	dBm	= decibel referred to 1 mW	DTL	= diode transistor logic
AMPL	= amplifier	ccw	= counterclockwise	dc	= direct current	DVM	= digital voltmeter
APC	= automatic phase control	CER	= ceramic	deg	= degree (temperature interval or difference)	ECL	= emitter coupled logic
ASSY	= assembly	CHAN	= channel	..°	= degree (plane angle)	EMF	= electromotive force
AUX	= auxiliary	cm	= centimeter	°C	= degree Celsius (centigrade)	EDP	= electronic data processing
avg	= average	CMO	= coaxial	°F	= degree Fahrenheit	ELECT	= electrolytic
AWG	= american wire gauge	COEF	= coefficient				
BAL	= balance	COM	= common				

ABBREVIATIONS (CONTINUED)

ENCAP	= encapsulated
EXT	= external
F	= farad
FET	= field-effect transistor
F/F	= flip-flop
FH	= flat head
FOL H	= fillister head
FM	= frequency modulation
FP	= front panel
FREQ	= frequency
FXD	= fixed
g	= gram
GE	= germanium
GHz	= gigahertz
GL	= glass
GND	= ground(ed)
H	= henry
h	= hour
HET	= heterodyne
HEX	= hexagonal
HD	= head
HDW	= hardware
HF	= high frequency
HG	= mercury
HI	= high
HP	= Hewlett-Packard
HPF	= high pass filter
HR	= hour (used in parts list)
HV	= high voltage
Hz	= Hertz
IC	= integrated circuit
ID	= inside diameter
IF	= intermediate frequency
IMPG	= impregnated
in	= inch
INCD	= incandescent
INCL	= include(s)
INP	= input
INS	= insulation
INT	= internal
kg	= kilogram
kHz	= kilohertz
kΩ	= kilohm
kV	= kilovolt
lb	= pound
LC	= inductance-capacitance
LED	= light-emitting diode
LF	= low frequency
LG	= long
LH	= left hand
LIM	= limit
LIN	= linear taper (used in parts list)
lin	= linear
LK WASH	= lockwasher
LO	= low; local oscillator
LOG	= logarithmic taper (used in parts list)
log	= logarithm(ic)
LPF	= low pass filter
LV	= low voltage
m	= meter (distance)
mA	= milliampere
MAX	= maximum
MΩ	= megohm
MEG	= meg (10^6) (used in parts list)
MET FLM	= metal film
MET OX	= metal oxide
MF	= medium frequency; microfarad (used in parts list)
MFR	= manufacturer
mg	= milligram
MHz	= megahertz
mH	= millihenry
mho	= mho
MIN	= minimum
min	= minute (time)
′	= minute (plane angle)
MINAT	= miniature
mm	= millimeter
MOD	= modulator
MOM	= momentary
MOS	= metal-oxide semiconductor
ms	= millisecond
MTG	= mounting
MTR	= meter (indicating device)
mV	= millivolt
mVac	= millivolt, ac
mVdc	= millivolt, dc
mVpk	= millivolt, peak
mVp-p	= millivolt, peak-to-peak
mVrms	= millivolt, rms
mW	= milliwatt
MUX	= multiplex
MY	= mylar
μA	= microampere
μF	= microfarad
μH	= microhenry
μmho	= micromho
μs	= microsecond
μV	= microvolt
μVac	= microvolt, ac
μVdc	= microvolt, dc
μVpk	= microvolt, peak
μVp-p	= microvolt, peak-to-peak
μVrms	= microvolt, rms
μW	= microwatt
nA	= nanoampere
NC	= no connection
N/C	= normally closed
NE	= neon
NEG	= negative
nF	= nanofarad
NI PL	= nickel plate
N/O	= normally open
NOM	= nominal
NORM	= normal
NPN	= negative-positive-negative
NPO	= negative-positive zero (zero temperature coefficient)
NRFR	= not recommended for field replacement
NSR	= not separately replaceable
ns	= nanosecond
nW	= nanowatt
OBD	= order by description
OD	= outside diameter
OH	= oval head
OP AMPL	= operational amplifier
OPT	= option
OSC	= oscillator
OX	= oxide
oz	= ounce
Ω	= ohm
P	= peak (used in parts list)
PAM	= pulse-amplitude modulation
PC	= printed circuit
PCM	= pulse-code modulation, pulse-count modulation
PDM	= pulse-duration modulation
pF	= picofarad
PH BRZ	= phosphor bronze
PHL	= Phillips
PIN	= positive-instrinsic-negative
PIV	= peak inverse voltage
pk	= peak
PL	= phase lock
PLO	= phase lock oscillator
PM	= phase modulation
PNP	= positive-negative-positive
P/O	= part of
POLY	= polystyrene
PORC	= porcelain
POS	= positive, position(s) (used in parts list)
POSN	= position
POT	= potentiometer
p-p	= peak-to-peak
PP	= peak-to-peak (used in parts list)
PPM	= pulse-position modulation
PREAMPL	= preamplifier
PRF	= pulse-repetition frequency
PRR	= pulse repetition rate
ps	= picosecond
PT	= point
PTM	= pulse-time modulation
PWM	= pulse-width modulation
PWV	= peak working voltage
RC	= resistance capacitance
RECT	= rectifier
REF	= reference
REG	= regulated
REPL	= replaceable
RF	= radio frequency
RFI	= radio frequency interference
RH	= round head; right hand
RLC	= resistance-inductance-capacitance
RMO	= rack mount only
rms	= root-mean-square
RND	= round
ROM	= read-only memory
R&P	= rack and panel
RWV	= reverse working voltage
S	= scattering parameter
s	= second (time)
″	= second (plane angle)
S-B	= slow-blow (fuse (used in parts list)
SCR	= silicon controlled rectifier; screw
SE	= selenium
SECT	= sections
SEMICON	= semiconductor
SHF	= superhigh frequency
SI	= silicon
SIL	= silver
SL	= slide
SNR	= signal-to-noise ratio
SPDT	= single-pole, double-throw
SPG	= spring
SR	= split ring
SPST	= single-pole, single-throw
SSB	= single sideband
SST	= stainless steel
STL	= steel
SQ	= square
SWR	= standing-wave ratio
SYNC	= synchronize
T	= timed (slow-blow fuse)
TA	= tantalum
TC	= temperature compensating
TD	= time delay
TERM	= terminal
TFT	= thin-film transistor
TGL	= toggle
THD	= thread
THRU	= through
TI	= titanium
TOL	= tolerance
TRIM	= trimmer
TSTR	= transistor
TTL	= transistor-transistor logic
TV	= television
TVI	= television interference
TWT	= traveling wave tube
U	= micro (10^{-6}) (used in parts list)
UF	= microfarad (used in parts list)
UHF	= ultrahigh frequency
UNREG	= unregulated
V	= volt
VA	= voltampere
Vac	= volts ac
VAR	= variable
VCO	= voltage-controlled oscillator
Vdc	= volts dc
VDCW	= volts dc, working (used in parts list)
V(F)	= volts, filtered
VFO	= variable-frequency oscillator
VHF	= very-high frequency
Vpk	= volts peak
Vp-p	= Volts peak-to-peak
Vrms	= volts rms
VSWR	= voltage standing wave ratio
VTO	= voltage-tuned oscillator
VTVM	= vacuum-tube voltmeter
V(X)	= volts, switched
W	= watt
W/	= with
WIV	= working inverse voltage
WW	= wirewound
W/O	= without
YIG	= yttrium-iron-garnet
Zo	= characteristic impedance

NOTE

All abbreviations in the parts list will be in upper case

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

6–3. ORDERING INFORMATION

6–4. To obtain replacement parts, address order of inquiry to your local Hewlett-Packard Sales and Service Office (see lists at rear of this manual for addresses). Identify parts by their Hewlett-Packard part numbers.

a. Instrument model number.
b. Instrument serial number.
c. Description of the part.
d. Function and location of the part.

6–5. HP PART NUMBER ORGANIZATION

6–6. Following is a general description of the HP part number system.

6–7. Component Parts and Materials

6–8. Generally, the prefix of HP part numbers identifies the type of device. Eight digit part numbers are used, where the four digit prefix identifies the type of component, part, or material and the four digit suffix indicates the specific type. Following is a list of some of the more commonly used prefixes for component parts. The list includes HP manufactured parts and purchased parts.

Prefix	Component/Part/Material
0121–	Capacitors, Variable (mechanical)
0122–	Capacitors, Voltage Variable (semiconductor)
0140–	Capacitors, Fixed } Non-Electrolytic
0150–	Capacitors, Fixed } Non-Electrolytic
0160–	Capacitors, Fixed } Non-Electrolytic
0180–	Capacitors, Fixed Electrolytic
0330–	Insulating Materials
0340–	Insulators, Formed
0370–	Knobs, Control
0380–	Spacers and Standoffs
0410–	Crystals
0470–	Adhesives
0490–	Relays
0510–	Fasteners
0674– thru 0778–	Resistors, Fixed (non wire wound)
0811– thru 0831–	Resistors (wire wound)
1200–	Sockets for components
1205–	Heat Sinks
1250–	Connectors (RF and related parts)
1251–	Connectors (non RF and related parts)
1410–	Bearings and Bushings
1420–	Batteries
1820–	Monolithic Digital Integrated Circuits
1826–	Monolithic Linear Integrated Circuits
1850–	Transistors, Germanium PNP
1851–	Transistors, Germanium NPN
1853–	Transistors, Silicon PNP
1854–	Transistors, Silicon NPN
1855–	Field-Effect-Transistors
1900– thru 1912–	Diodes

Prefix	Component/Part/Material
1920- thru 1952-	Vacuum Tubes
1990-	Semiconductor Photosensitive and Light-Emitting Diodes
3100- thru 3106-	Switches
8120-	Cables
9100-	Transformers, Coils, Chokes, Inductors, and Filters

6-9. For example, 1854-0037, 1854-0221, and 1851-0192 are all NPN transistors. The first two are silicon and the last is germanium.

6-10. General Usage Parts

6-11. The following list gives the prefixes for HP manufactured parts used in several instruments, e.g., side frames, feet, top and bottom covers, etc. These are eight-digit part numbers with the four-digit prefix identifying the type of parts as shown below:

Type of Part	Prefix
Sheet Metal	5000- to 5019-
Machined	5020- to 5039-
Molded	5040- to 5059-
Assemblies	5060- to 5079-
Components	5080- to 5099-

6-12. Specific Instrument Parts

6-13. These are HP manufactured parts for use in individual instruments or series of instruments. For these parts, the prefix indicates the instrument and the suffix indicates the type of part. For example, 05358-60001 is an assembly used in the 5358A. Following is a list of suffixes commonly used.

Type of Part	P/N Suffix
Sheet Metal	-00000 to -00499
Machined	-20000 to -20499
Molded	-40000 to -40499
Assembly	-60000 to -60499
Component	-80000 to -80299
Documentation	-90000 to -90249

Table 6-1. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	05358-60001	1	HP-IB INPUT ASSEMBLY	28480	05358-60001
A1J1	1251-1626	1	CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS	71785	252-12-30-300
A1J2	1200-0485	1	SOCKET-IC 14-PIN PC MOUNTING	28480	1200-0485
A1P1	1251-3283	1	CONNECTOR: 24-CONT; FEM; MICRORIBBON	28480	1251-3283
A1S1	3101-1973	1	SWITCH, SLIDE 7 SPST	11237	206 TYPE
A1W1	8159-0005	1	WIRE 22AWG W PVC 1X22 80C	28480	8159-0005
	1530-1098	2	FASTENER:0.136" DIA 6-32 THREAD	00000	OBD
A2	05358-60002	1	MOTHER BOARD ASSEMBLY	28480	05358-60002
A2J1	1200-0424	1	SOCKET-IC BLK 14 CONTACT	23880	CSA2900-14B
A2J2	1250-0836	1	CONNECTOR-RF SMC M PC	2K497	CD-700141
A2J3	1200-0423	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0423
A2P1	1251-0099	1	CONNECTOR 50-PIN M MICRO RIBBON	9D949	57-10500-375
A2XA3A	1251-1365	11	CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-300
A2XA3B	1251-1365		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-300
A2XA4A	1251-1365		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-300
A2XA4B	1251-1365		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-300
A2XA5	1251-1365		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-300
A2XA6	1251-1365		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-300
A2XA7	1251-1365		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-300
A2XA8	1251-1365		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-300
A2XA9	1251-1365		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-300
A2XA10	1251-1365		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-300
A2XA11	1251-1365		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-300
	0360-0124	45	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
	0380-0789	6	STANDOFF-RVT-ON 1.75LG 6-32THD .2500 BRS	06540	9550-C-6-0632
A3	05358-60003	1	HP-IB CONTROL ASSEMBLY	28480	05358-60003
A3C1	0160-3879	64	CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C2	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C3	0140-0234	6	CAPACITOR-FXD 500PF +-1% 300WVDC MICA	72136	DM15F501F0300WV1C
A3C4	0180-1701	13	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A3C5	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C6	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C7	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C8	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C9	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C10	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C11	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C12	0140-0234		CAPACITOR-FXD 500PF +-1% 300WVDC MICA	72136	DM15F501F0300WV1C
A3C13	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C14	0140-0234		CAPACITOR-FXD 500PF +-1% 300WVDC MICA	72136	DM15F501F0300WV1C
A3C15	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C16	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C17	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C18	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A3C19	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C20	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C21	0140-0205	1	CAPACITOR-FXD 62PF +-5% 300WVDC MICA	72136	DM15E620J0300WV1CR
A3C22	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3C23	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A3CR1	1901-0040	13	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3CR2	1901-0535	15	DIODE-SCHOTTKY	28480	1901-0535
A3CR3	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A3L1	9100-1788	5	COIL: FXD; NON-MOLDED RF CHOKE; .75UH	02114	VK200-20/4B
A3L2	9100-1788		COIL: FXD; NON-MOLDED RF CHOKE; .75UH	02114	VK200-20/4B
A3R1	1810-0135	1	NETWORK-RES 6-PIN-SIP .15-PIN-SPCG	28480	1810-0135
A3R2	0683-4715	1	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A3R3	0757-0280	14	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R4	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R5	0757-0416	9	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A3TP1	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A3TP2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A3TP3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A3TP4	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A3TP5	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124

See introduction to this section for ordering information

Table 6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A3TP6	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A3TP7	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A3U1	1820-1419	1	IC-DIGITAL SN74LS85N TTL LS MAGTD	01295	SN74LS85N
A3U2	1820-1689	4	IC-DIGITAL MC3446P QUAD	04713	MC3446P
A3U3	1820-1689		IC-DIGITAL MC3446P QUAD	04713	MC3446P
A3U4	1820-1202	6	IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
A3U5	1820-1689		IC-DIGITAL MC3446P QUAD	04713	MC3446P
A3U6	1820-1689		IC-DIGITAL MC3446P QUAD	04713	MC3446P
A3U7	1820-1199	13	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A3U8	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A3U9	1820-1201	4	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
A3U10	1820-1204	2	IC-DIGITAL SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
A3U11	1820-1204		IC-DIGITAL SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
A3U12	1820-1282	3	IC-DIGITAL SN74LS109N TTL LS DUAL	01295	SN74LS109N
A3U13	1820-1144	16	IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A3U14	1820-1281	1	IC-DIGITAL SN74LS139N TTL LS DUAL 2	01295	SN74LS139N
A3U15	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A3U16	1820-1212	1	IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN74LS112N
A3U17	1820-1282		IC-DIGITAL SN74LS109N TTL LS DUAL	01295	SN74LS109N
A3U18	1820-1197	18	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U19	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
A3U20	1820-1205	1	IC-DIGITAL SN74LS21N TTL LS DUAL 4 AND	01295	SN74LS21N
A3U21	1820-1216	3	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
A3U22	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A3U23	1820-1195	7	IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
A3U24	1820-1216		IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
A3U25	1820-1210	1	IC-DIGITAL SN74LS51N TTL LS DUAL 2	01295	SN74LS51N
A3U26	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U27	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U28	1820-1759	3	IC, DIGITAL TTL	28480	1820-1759
A3U29	1820-1202		IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
A3U30	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A3U31	1820-1206	8	IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
A3U32	1820-1211	5	IC-DIGITAL SN74LS86N TTL LS QUAD 2	01295	SN74LS86N
A3U33	1820-1440	2	IC-DIGITAL SN74LS279N TTL LS QUAD	01295	SN74LS279N
A3U34	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U35	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U36	1820-1112	13	IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A3U37	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U38	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U39	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A3U40	1820-1282		IC-DIGITAL SN74LS109N TTL LS DUAL	01295	SN74LS109N
A3U41	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A3U42	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A3U43	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
A3U44	1820-1194	2	IC-DIGITAL SN74LS193N TTL LS BIN	01295	SN74LS193N
A3U45	1820-1759		IC, DIGITAL TTL	28480	1820-1759
A3U46	1818-0640	2	IC 6561N 64-BIT RAM TTL	50364	6561N
A3U47	1820-1759		IC, DIGITAL TTL	28480	1820-1759
A3U48	1818-0640		IC 6561N 64-BIT RAM TTL	50364	6561N
A3U49	1820-1206		IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
A3U50	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
A3U51	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A3U52	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A3U53	1820-1279	2	IC-DIGITAL SN74LS190N TTL LS DECD	01295	SN74LS190N
A3U54	1820-1202		IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
A3U55	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U56	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A3U57	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U58	1820-1279		IC-DIGITAL SN74LS190N TTL LS DECD	01295	SN74LS190N
A3U59	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A3U60	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A3U61	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U62	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U63	1820-1206		IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
A3U64	1820-1206		IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
A3U65	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A3U66	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
A3U67	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A3U68	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A3U69	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A3U70	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A3U71	1820-1211		IC-DIGITAL SN74LS86N TTL LS QUAD 2	01295	SN74LS86N

See Introduction to this section for ordering information

Table 6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			A3 MISCELLANEOUS		
	1480-0116	6	EXTRACTOR PIN:1/16" DIA	73957	GP24-063X250-12
	5000-9043	6	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-1464	7	EXTRACTOR, P.C.	28480	5040-1464
	5040-6843	5	EXTRACTOR, P.C. BOARD	28480	5040-6843
A4	05358-60004	1	MEMORY CONTROL ASSEMBLY	28480	05358-60004
A4C1	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A4C2	0180-0106	1	CAPACITOR-FXD 68UF+-20% 6VDC TA	56289	150D686X0006B2
A4C3	0140-0234		CAPACITOR-FXD 500PF +-1% 300WVDC MICA	72136	DM15F501F0300WV1C
A4C4	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C5	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C6	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A4C7	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C8	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C9	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A4C10	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C11	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C12	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C13	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C14	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C15	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C16	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C17	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C18	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C19	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C20	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C21	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C22	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A4C23	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A4C24	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A4CR1	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A4CR2	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A4CR3	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A4CR4	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A4CR5	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A4CR6	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A4Q1	1853-0036	4	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4Q2	1853-0036		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4Q3	1854-0215	9	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A4Q4	1854-0092	2	TRANSISTOR NPN SI PD=200MW FT=600MHZ	28480	1854-0092
A4Q5	1854-0092		TRANSISTOR NPN SI PD=200MW FT=600MHZ	28480	1854-0092
A4R1	0757-0274	4	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A4R2	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R3	0757-0427	4	RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A4R4	0757-0279	1	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A4R5	0757-0427		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A4R6	0757-0274		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A4R7	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R8	0757-0278	1	RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A4R9	0757-0283	8	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A4R10	0757-0283		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A4R11	0757-0283		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A4R12	0757-0283		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A4R13	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R14	0757-0394	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A4R15	0757-0442	3	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R16	0757-0442		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R17	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R18	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R19	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R20	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4TP1	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP4	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP5	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP6	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP7	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP8	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP9	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP10	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124

Table 6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A4TP11	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP12	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP13	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP14	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4TP15	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A4U1	1820-1425	1	IC-DIGITAL SN74LS132N TTL LS QUAD 2 NAND	01295	SN74LS132N
A4U2	1820-1251	2	IC-DIGITAL SN74LS196N TTL LS DECD	01295	SN74LS196N
A4U3	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A4U4	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A4U5	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A4U6	1820-1112		IC-DIGITAL SN74L874N TTL LS DUAL	01295	SN74LS74N
A4U7	1820-1433	1	IC-DIGITAL SN74LS164N TTL LS R-S	01295	SN74LS164N
A4U8	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A4U9	1820-1202		IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
A4U10	1820-0693	2	IC-DIGITAL SN7874N TTL S DUAL	01295	SN74S74N
A4U11	1820-1206		IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
A4U12	1820-0683	1	IC-DIGITAL SN74S04N TTL LS HEX 1	01295	SN74S04N
A4U13	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A4U14	1820-1440		IC-DIGITAL SN74LS279N TTL LS QUAD	01295	SN74LS279N
A4U15	1820-1444	6	IC-DIGITAL SN74LS298N TTL LS QUAD 2	01295	SN74LS298N
A4U16	1820-0578	2	IC-DIGITAL DM8551N TTL QUAD D-TYPE	27014	DM8551N
A4U17	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
A4U18	1820-1444		IC-DIGITAL SN74LS298N TTL LS QUAD 2	01295	SN74LS298N
A4U19	1820-0578		IC-DIGITAL DM8551N TTL QUAD D-TYPE	27014	DM8551N
A4U20	1820-1464	4	IC-DIGITAL SN74393N TTL DUAL BIN	01295	SN74393N
A4U21	1820-1444		IC-DIGITAL SN74LS298N TTL LS QUAD 2	01295	SN74LS298N
A4U22	1820-1250	2	IC-DIGITAL DM8095N TTL HEX 1 NON-INV	27014	DM8095N
A4U23	1820-1464		IC-DIGITAL SN74393N TTL DUAL BIN	01295	SN74393N
A4U24	1820-1444		IC-DIGITAL SN74LS298N TTL LS QUAD 2	01295	SN74LS298N
A4U25	1820-1250		IC-DIGITAL DM8095N TTL HEX 1 NON-INV	27014	DM8095N
A4U26	1820-1464		IC-DIGITAL SN74393N TTL DUAL BIN	01295	SN74393N
A4U27	1820-1444		IC-DIGITAL SN74LS298N TTL LS QUAD 2	01295	SN74LS298N
A4U28	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A4U29	1820-1464		IC-DIGITAL SN74393N TTL DUAL BIN	01295	SN74393N
A4U30	1820-1444		IC-DIGITAL SN74LS298N TTL LS QUAD 2	01295	SN74LS298N
A4U31	1820-1245	1	IC-DIGITAL SN74LS155N TTL LS DUAL 2	01295	SN74LS155N
A4U32	1820-1244	3	IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
A4U33	1820-1244		IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
A4U34	1820-1208	1	IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
A4U35	1820-1244		IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
A4U36	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
A4U37	1820-0987	1	IC-DIGITAL 93L18PC TTL L B	01295	93L18PC
A4U38	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
A4U39	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A4U40	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A4U41	1820-1435	4	IC-DIGITAL SN74LS169N TTL LS BIN	01295	SN74LS169N
A4U42	1820-1435		IC-DIGITAL SN74LS169N TTL LS BIN	01295	SN74LS169N
A4U43	1820-1207	1	IC-DIGITAL SN74LS30N TTL LS 8 NAND	01295	SN74LS30N
A4U44	1820-1435		IC-DIGITAL SN74LS169N TTL LS BIN	01295	SN74LS169N
A4U45	1820-1435		IC-DIGITAL SN74LS169N TTL LS BIN	01295	SN74LS169N
			A4 MISCELLANEOUS		
	1480-0116		EXTRACTOR PIN:1/16" DIA	73957	GP24-063X250-12
	5000-9043		PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-1464		EXTRACTOR:CARD	28480	5040-1464
	5040-6843		EXTRACTOR, P.C. BOARD	28480	5040-6843
A5	05358-60005	1	SYSTEM CONTROL ASSEMBLY	28480	05358-60005
A5C1	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A5C2	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A5C3	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A5C4	0140-0234		CAPACITOR-FXD 500PF +-1% 300WVDC MICA	72136	DM15F501F0300WV1C
A5C5	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A5C6	0140-0234		CAPACITOR-FXD 500PF +-1% 300WVDC MICA	72136	DM15F501F0300WV1C
A5C7	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A5C8	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A5C9	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A5C10	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A5C11	0160-2308	1	CAPACITOR-FXD 36PF +-5% 300WVDC MICA	28480	0160-2308
A5C12	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A5C13	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A5CR1	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A5CR2	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A5CR3	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A5CR4	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A5CR5	1901-0535		DIODE-SCHOTTKY	28480	1901-0535

Table 6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A5CR6	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A5L1	9100-1788		COIL; FXD; NON-MOLDED RF CHOKE; .75UH	02114	VK200-20/4B
A5Q1	1854-0071	5	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A5Q2	1854-0215		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A5Q3	1854-0094	2	TRANSISTOR NPN SI PD=200MW FT=350MHZ	28480	1854-0094
A5Q4	1854-0215		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A5R1	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-5110-F
A5R2	0757-0316	1	RESISTOR 42.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-42R2-F
A5R3	0757-0465	6	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A5R4	0757-0283		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A5R5	0757-0442		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R6	0757-0283		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A5R7	0757-1094	2	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A5R8	0698-0082	2	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A5R9	0698-3437	1	RESISTOR 133 1% .125W F TC=0+-100	24546	C4-1/8-T0-133R-F
A5R10	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A5R11	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A5R12	0757-1094		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A5R13	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A5R14	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R15	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A5R16	0757-0428	1	RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
A5TP1	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A5TP2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A5TP3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A5TP4	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A5TP5	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A5TP6	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A5TP7	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A5TP8	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A5U1	1820-1206		IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
A5U2	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A5U3	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A5U4	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A5U5	1820-1277	9	IC-DIGITAL SN74LS192N TTL LS DECD	01295	SN74LS192N
A5U6	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A5U7	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A5U8	1820-1277		IC-DIGITAL SN74LS192N TTL LS DECD	01295	SN74LS192N
A5U9	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A5U10	1820-1206		IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
A5U11	1820-1202		IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
A5U12	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A5U13	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A5U14	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A5U15	1820-1277		IC-DIGITAL SN74LS192N TTL LS DECD	01295	SN74LS192N
A5U16	1820-1196	5	IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
A5U17	1820-1211		IC-DIGITAL SN74LS86N TTL LS QUAD 2	01295	SN74LS86N
A5U18	1820-1277		IC-DIGITAL SN74LS192N TTL LS DECD	01295	SN74LS192N
A5U19	1820-1196		IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
A5U20	1820-1729	1	IC-DIGITAL SN74LS259N TTL LS COM	01295	SN74LS259N
A5U21	1820-1277		IC-DIGITAL SN74LS192N TTL LS DECD	01295	SN74LS192N
A5U22	1820-1196		IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
A5U23	1820-1277		IC-DIGITAL SN74LS192N TTL LS DECD	01295	SN74LS192N
			A5 MISCELLANEOUS		
	1480-0116		EXTRACTOR PIN;1/16" DIA	73957	GP24-063X250-12
	5000-9043		PINIP.C. BOARD EXTRACTOR	28480	5000-9043
	5040-1464		EXTRACTOR;CARD	28480	5040-1464
	5040-6852	1	EXTRACTOR, ORANGE	28480	5040-6852
A6	05358-60006	1	GATE CONTROL ASSEMBLY	28480	05358-60006
A6C1	0160-3879		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C2	0160-3879		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C3	0160-3879		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C4	0160-3879		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C5	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A6C6	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A6C7	0160-3879		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C8	0160-3879		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C9	0140-0198	1	CAPACITOR-FXD 200PF +-5% 300WVDC MICA	72136	DM15F201J0300WV1CR
A6C10	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879

See introduction to this section for ordering information

Table 6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A6C11	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A6C12	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A6C13	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A6C14	0180-0116	1	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X903582
A6C15	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X000642
A6C16	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A6C17	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A6C18	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A6C19	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A6C20	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A6CR1	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A6CR2	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A6CR3	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A6CR4	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A6CR5	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A6CR6	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A6CR7	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A6L1	9100-1788		COIL, FXD, NON-MOLDED RF CHOKE, .75UH	02114	VK200-20/4B
A6Q1	1854-0215		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A6Q2	1854-0094		TRANSISTOR NPN SI PD=200MW FT=350MHZ	28480	1854-0094
A6Q3	1854-0215		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A6Q4	1854-0215		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A6Q5	1853-0015	3	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
A6Q6	1854-0215		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A6Q7	1853-0015		TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
A6Q8	1854-0215		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A6Q9	1854-0215		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A6Q10	1853-0015		TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
A6R1	0757-0427		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A6R2	0757-0427		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A6R3	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R4	0757-0403	1	RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
A6R5	0757-0401	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R6	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R7	0698-0082		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A6R8	0757-0419	1	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A6R9	0698-3446	2	RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A6R10	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R11	0698-0084	3	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R12	0698-0084		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R13	0757-0465		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R14	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R15	0698-3154	1	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A6R16	0698-3153	2	RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A6R17	0757-0274		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A6R18	0698-3440	1	RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A6R19	0757-0420	1	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A6R20	0698-3446		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A6R21	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R22	0757-0400	1	RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A6R23	0757-0274		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A6R24	0698-3153		RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A6R25	0757-0421	2	RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-825R-F
A6R26	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R27	0698-5180	4	RESISTOR 2K 5% .125W CC TC=-350/+857	01121	BB2025
A6R28	0698-5180		RESISTOR 2K 5% .125W CC TC=-350/+857	01121	BB2025
A6R29	0698-5180		RESISTOR 2K 5% .125W CC TC=-350/+857	01121	BB2025
A6R30	0698-5180		RESISTOR 2K 5% .125W CC TC=-350/+857	01121	BB2025
A6R31	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R32	0757-0283		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A6R33	0757-0283		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A6TP1	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A6TP2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A6TP3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A6TP4	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A6TP5	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A6TP6	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A6U1	1820-1211		IC-DIGITAL SN74LS86N TTL LS QUAD 2	01295	SN74LS86N
A6U2	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A6U3	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A6U4	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A6U5	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N

See Introduction to this section for ordering information

Table 6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A6U6	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A6U7	1820-1211		IC-DIGITAL SN74LS86N TTL LS QUAD 2	01295	SN74LS86N
A6U8	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A6U9	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A6U10	1820-1251		IC-DIGITAL SN74LS196N TTL LS DECD	01295	SN74LS196N
A6U11	1820-0693		IC-DIGITAL SN74S74N TTL S DUAL	01295	SN74S74N
A6U12	1820-1206		IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
A6U13	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX I	01295	SN74LS04N
A6U14	1820-1180	1	IC-DIGITAL MOS	50088	MK5009P
A6U15	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
A6U16	1820-1216		IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
A6U17	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
A6U18	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A6U19	1820-1277		IC-DIGITAL SN74LS192N TTL LS DECD	01295	SN74LS192N
A6U20	1820-1196		IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
A6U21	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A6U22	1820-1277		IC-DIGITAL SN74LS192N TTL LS DECD	01295	SN74LS192N
A6U23	1820-1196		IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
A6U24	1820-1194		IC-DIGITAL SN74LS193N TTL LS BIN	01295	SN74LS193N
A6U25	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
A6U26	1820-1277		IC-DIGITAL SN74LS192N TTL LS DECD	01295	SN74LS192N
			A6 MISCELLANEOUS		
	5000-9043		PINEP.C. BOARD EXTRACTOR	28480	5000-9043
	5040-1464		EXTRACTOR1CARD	28480	5040-1464
	5040-6843		EXTRACTOR, P.C. BOARD	28480	5040-6843
A7	05358-60007	1	CONVERTER ASSEMBLY	28480	05358-60007
A7C1	0180-0428	2	CAPACITOR-FXD 68UF+-20% 6VDC TA	28480	0180-0428
A7C2	0160-4084	1	CAPACITOR-FXD .1UF +-20% 50WVDC CER	28480	0160-4084
A7C3	0180-0651	2	CAPACITOR-FXD 1700UF+75-10% 10VDC AL	09023	UFT-1700-10
A7C4	0180-1943	2	CAPACITOR-FXD 1000UF+75-10% 25VDC AL	56289	39D108G025GL4
A7C5	0180-1943		CAPACITOR-FXD 1000UF+75-10% 25VDC AL	56289	39D108G025GL4
A7C6	0180-0651		CAPACITOR-FXD 1700UF+75-10% 10VDC AL	09023	UFT-1700-10
A7C7	0160-3455	1	CAPACITOR-FXD 470PF +-10% 1000WVDC CER	28480	0160-3455
A7C8	0180-0428		CAPACITOR-FXD 68UF+-20% 6VDC TA	28480	0180-0428
A7CR1	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A7CR2	1902-0558	4	DIODE-ZNR 12V 5% DO-15 PD=1W TC=+.074%	28480	1902-0558
A7CR3	1902-0558		DIODE-ZNR 12V 5% DO-15 PD=1W TC=+.074%	28480	1902-0558
A7CR4	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A7CR5	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A7CR6 *	1901-0784	2	DIODE-HOT CARRIER	28480	1901-0784
A7CR7	1902-0522	2	DIODE-ZNR 1N5340B 6V 5% PD=5W IR=1UA	04713	1N5340B
A7CR8 *	1901-0784		DIODE-HOT CARRIER	28480	1901-0784
A7CR9	1902-0522		DIODE-ZNR 1N5340B 6V 5% PD=5W IR=1UA	04713	1N5340B
A7CR10	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
			*EARLY VERSIONS CONTAIN PN 1901-0676		
A7CR11	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A7CR12	1902-0558		DIODE-ZNR 12V 5% DO-15 PD=1W TC=+.074%	28480	1902-0558
A7CR13	1902-0558		DIODE-ZNR 12V 5% DO-15 PD=1W TC=+.074%	28480	1902-0558
A7CR14	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A7DS1	1990-0327	2	LED-VISIBLE LUM-INT=800UCD IF=50MA-MAX	28480	1990-0327
A7DS2	1990-0327		LED-VISIBLE LUM-INT=800UCD IF=50MA-MAX	28480	1990-0327
A7L1	9100-3017	2	INDUCTOR	28480	9100-3017
A7L2	9100-3060	2	COIL/INDUCTOR	28480	9100-3060
A7L3	9100-3060		COIL/INDUCTOR	28480	9100-3060
A7L4	9100-3017		INDUCTOR	28480	9100-3017
A7Q1	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q2	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q3	1853-0036		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A7Q4	1853-0363	2	TRANSISTOR PNP SI PD=50W	03508	D45HS
A7Q5	1853-0363		TRANSISTOR PNP SI PD=50W	03508	D45HS
A7Q6	1853-0036		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A7Q7	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q8	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7R1	0683-8215	1	RESISTOR 820 5% .25W FC TC=-400/+600	01121	CB8215
A7R2	0683-3015	1	RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A7R3	0683-1025	4	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A7R4	0683-2425	2	RESISTOR 2.4K 5% .25W FC TC=-400/+700	01121	CB2425
A7R5	0683-1515	2	RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A7R6	0683-5125	4	RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A7R7	0683-5145	2	RESISTOR 510K 5% .25W FC TC=-800/+900	01121	CB5145
A7R8	0686-3615	1	RESISTOR 360 5% .5W CC TC=0+529	01121	EB3615
A7R9	0683-5125		RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A7R10	0683-5115	2	RESISTOR 510 5% .25W FC TC=-400/+600	01121	CB5115

Table 6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A7R11	0757-0465		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A7R12	0698-3159	2	RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
A7R13	0698-3449	2	RESISTOR 28.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2872-F
A7R14	0757-0465		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A7R15	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A7R16	0698-0084		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A7R17	0683-5115		RESISTOR 510 5% .25W FC TC=-400/+600	01121	CB5115
A7R18	0683-5125		RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A7R19	0686-7505	1	RESISTOR 75 5% .5W CC TC=0+912	01121	EB7505
A7R20	0757-0421		RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-8250-F
A7R21	0683-5145		RESISTOR 510K 5% .25W FC TC=-800/+900	01121	CB5145
A7R22	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A7R23	0757-0465		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A7R24	0698-3449		RESISTOR 28.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2872-F
A7R25	0698-3159		RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
A7R26	0683-1515		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A7R27	0757-0465		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A7R28	0683-3015		RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A7R29	0683-3015		RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A7R30	0683-2425		RESISTOR 2.4K 5% .25W FC TC=-400/+700	01121	CB2425
A7R31	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A7R32	0683-5125		RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A7TP1	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A7TP2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A7TP3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A7TP4	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
A7U1	1820-0477	2	IC LM 301A OP AMP	27014	LM301AN
A7U2	1820-0493	2	IC LM 307 OP AMP	27014	LM307N
A7U3	1820-0477		IC LM 301A OP AMP	27014	LM301AN
A7U4	1820-0493		IC LM 307 OP AMP	27014	LM307N
			A7 MISCELLANEOUS		
	1480-0118		EXTRACTOR PIN;1/16" DIA	73957	GP20-063X250-12
	5000-9043		PIN;P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-1464		EXTRACTOR;CARD	28480	5040-1464
	5040-6843		EXTRACTOR, P.C. BOARD	28480	5040-6843
A8	05358-60008	4	MEMORY ASSEMBLY	28480	05358-60008
A8C1	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A8C2	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A8C3	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A8C4	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A8C5	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A8C6	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A8C7	0180-0229	1	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	1500336X9010B2
A8C8	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A8C9	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A8L1	9100-1788		COIL; FXD; NON-MOLDED RF CHOKE; .75UH	02114	VK200-20/4B
A8U1	1818-0198	16	IC, MOS 1KX1 RAM	28480	1818-0198
A8U2	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U3	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U4	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U5	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U6	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U7	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U8	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U11	1820-1202		IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
A8U12	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U13	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U14	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U15	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U16	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
A8U17	1818-0198		IC, MOS 1KX1 RAM	28480	1818-0198
			A8 MISCELLANEOUS		
	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
	5000-9043		PIN;P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6843		EXTRACTOR, P.C. BOARD	28480	5040-6843
A9	05358-60008		MEMORY ASSEMBLY (OPTION 001) (SAME AS A8)	28480	05358-60008

See Introduction to this section for ordering information

Table 6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A10	05358-60008		MEMORY ASSEMBLY (OPTION 001) (SAME AS A8)	28480	05358-60008
A11	05358-60008		MEMORY ASSEMBLY (OPTION 001) (SAME AS A8)	28480	05358-60008
A12	05358-60009	1	DISPLAY ASSEMBLY	28480	05358-60009
A12C1	0180-0155	1	CAPACITOR-FXD 2.2UF +-20% 20VDC TA	56289	1500225X0020A2
A12DS1	1990-0485	2	LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	1990-0485
A12DS2	1990-0485		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	1990-0485
A12DS3	1990-0486	1	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A12DS4	1990-0487	2	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0487
A12DS5	1990-0487		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0487
A12R1	0757-0407	5	RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A12R2	0757-0407		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A12R3	0757-0407		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A12R4	0757-0407		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A12R5	0757-0407		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A12U1	1820-0471	1	IC-DIGITAL SN7406N TTL HEX 1	01295	SN7406N
A12W1	8120-0616	1	CABLE ASSY 26AWG 16-CNDCT	28480	8120-0616
	05000-20017	5	SPACER, LED SINGLE	28480	05000-20017
A13	05358-60010	1	BNC IO ASSEMBLY	28480	05358-60010
A13J1	1250-1163	5	CONNECTOR-RF BNC FEM SGL-HOLE-RR 50-OHM	28480	1250-1163
A13J2	1250-1163		CONNECTOR-RF BNC FEM SGL-HOLE-RR 50-OHM	28480	1250-1163
A13J3	1250-1163		CONNECTOR-RF BNC FEM SGL-HOLE-RR 50-OHM	28480	1250-1163
A13J4	1250-1163		CONNECTOR-RF BNC FEM SGL-HOLE-RR 50-OHM	28480	1250-1163
A13J5	1250-1163		CONNECTOR-RF BNC FEM SGL-HOLE-RR 50-OHM	28480	1250-1163
A13W1	8120-2251	1	CABLE ASSY 28AWG 14-CNDCT	28480	8120-2251
			MISCELLANEOUS PARTS		
	05358-60100	2	CONNECTOR AND CABLE ASSEMBLY(REAR PANEL)	28480	05358-60100
	0890-0029		TUBING-NS .187-D/.093-RCVD .02-WALL	92194	FIT-221-3/16-BLK
	0890-0706		TUBING-NS .093-D/.046-RCVD .02-WALL	06090	RNF-100-3/32-BLK
	1200-0063	2	CONNECTOR-SGL CONT SKT #20	28480	1200-0063
	1250-0824	1	CONNECTOR-RF SMC FEM [illegible]D	24931	37P106-1
	1251-0179	1	INSERT-SUBMIN D CONN	71785	DM-53740-5001
	1251-2214	1	CONNECTOR 37-PIN [illegible] D SERIES	71785	DCM-37W5P
	8120-1946		CABLE-CO[illegible]X 50 OHM .1-OD 26AWG	28480	8120-1946
	8150-0007		WIRE 22AWG BR 300V PVC 7X30 BOC	28480	8150-0007
	8150-0022		WIRE 22AWG W 300V PVC 7X30 BOC	28480	8150-0022
	5020-0176	2	INSULATOR FOR SNAP-ON PINS	28480	5020-0176
	9211-0353	1	CARTON-PACKAGING	24840	9211-0353
			CABINET PARTS		
H1	0380-0644	2	STANDOFF-HEX 6/32"	00000	ORD
	1251-2205	1	POLARIZING KEY-PC EDGE CONN	71785	470-11-50-200
H2	1460-1186	1	WIREFORM 2.22-LG MOW	28480	1460-1186
	2190-0034	2	WASHER-LK HLCL NO.-10 .194-IN-ID	28480	2190-0034
	3050-0071	1	WASHER-FL MTLC NO.-8 .169-IN-ID	28480	3050-0071
MP1	05358-00001	1	PANEL, FRONT	28480	05358-00001
MP2	05358-00002	1	PANEL, REAR	28480	05358-00002
MP3	05358-00003	1	SIDE, LEFT	28480	05358-00003
MP4	05358-00004	1	SIDE, RIGHT	28480	05358-00004
MP5	05358-00005	1	COVER, TOP	28480	05358-00005
MP6	05358-20200	1	PANEL, SUB	28480	05358-20200
MP7	05358-20201	3	GUIDE, P.C. BOARD	28480	05358-20201
W1	05358-60100		CABLE ASSEMBLY, REAR PANEL	28480	05358-60100
MP8	08621-20051	1	HANDLE, DRAWER LATCH	28480	08621-20051
H3	08621-20052	1	SCREW, LATCH	28480	08621-20052
MP9	10590-00001	1	SPACER, CONNECTOR ALIGN	28480	10590-00001

See introduction to this section for ordering information

Table 6-2. Manufacturers Codes List

MFR NO.	MANUFACTURER NAME ADDRESS ZIP CODE
00000	NO M/F DESCRIPTION FOR THIS MFG NUMBER
01121	ALLEN-BRADLEY CO. MILWAUKEE WI 53212
01295	TEXAS INSTR INC SEMICOND CMPNT DIV. DALLAS TX 75231
02114	FERROXCUBE CORP. SAUGERTIES NY 12477
03508	GE CO SEMICONDUCTOR PROD DEPT. SYRACUSE NY 13201
04713	MOTOROLA SEMICONDUCTOR PRODUCTS PHOENIX AZ 85008
06090	RAYCHEM CORP. MENLO PARK CA 94025
06540	AMATOM ELEK HARDWARE DIV OF MITE NEW ROCHELLE NY 1802
07263	FAIRCHILD SEMICONDUCTOR DIV. MOUNTAIN VIEW CA 94040
09023	CORNELL-DUBILIER ELEK DIV FED PAC. SANFORD NC 27330
11237	CTS KEENE INC. PASO ROBLES CA 93446
2K497	CABLEWAVE SYSTEMS INC. NORTH HAVEN CT 06473
23880	STANFORD APPLIED ENGINEERING INC. SANTA CLARA CA 95050
24546	CORNING GLASS WORKS (BRADFORD) BRADFORD PA 16701
24931	SPECIALTY CONNECTOR CO INC. INDIANAPOLIS IN 46227
27014	NATIONAL SEMICONDUCTOR CORP. SANTA CLARA CA 95051
28480	HEWLETT-PACKARD CO CORPORATE HQ. PALO ALTO CA 94304
e0088	MOSTEK CORP. CARROLLTON TX 75006
50364	MONOLITHIC MEMORIES INC. SUNNYVALE CA 94086
56289	SPRAGUE ELECTRIC CO. NORTH ADAMS MA 01247
71785	TRW ELEK COMPONENTS CINCH DIV. ELK GROVE VILLAGE IL 60007
72136	ELECTRO MOTIVE CORP SUB IEC, WILLIMANTIC CT 06226
90949	AMPHENOL SALES DIV OF BUNKER-RAMO HAZELWOOD MO 63042
92194	ALPHA WIRE CORP. ELIZABETH NJ 07207

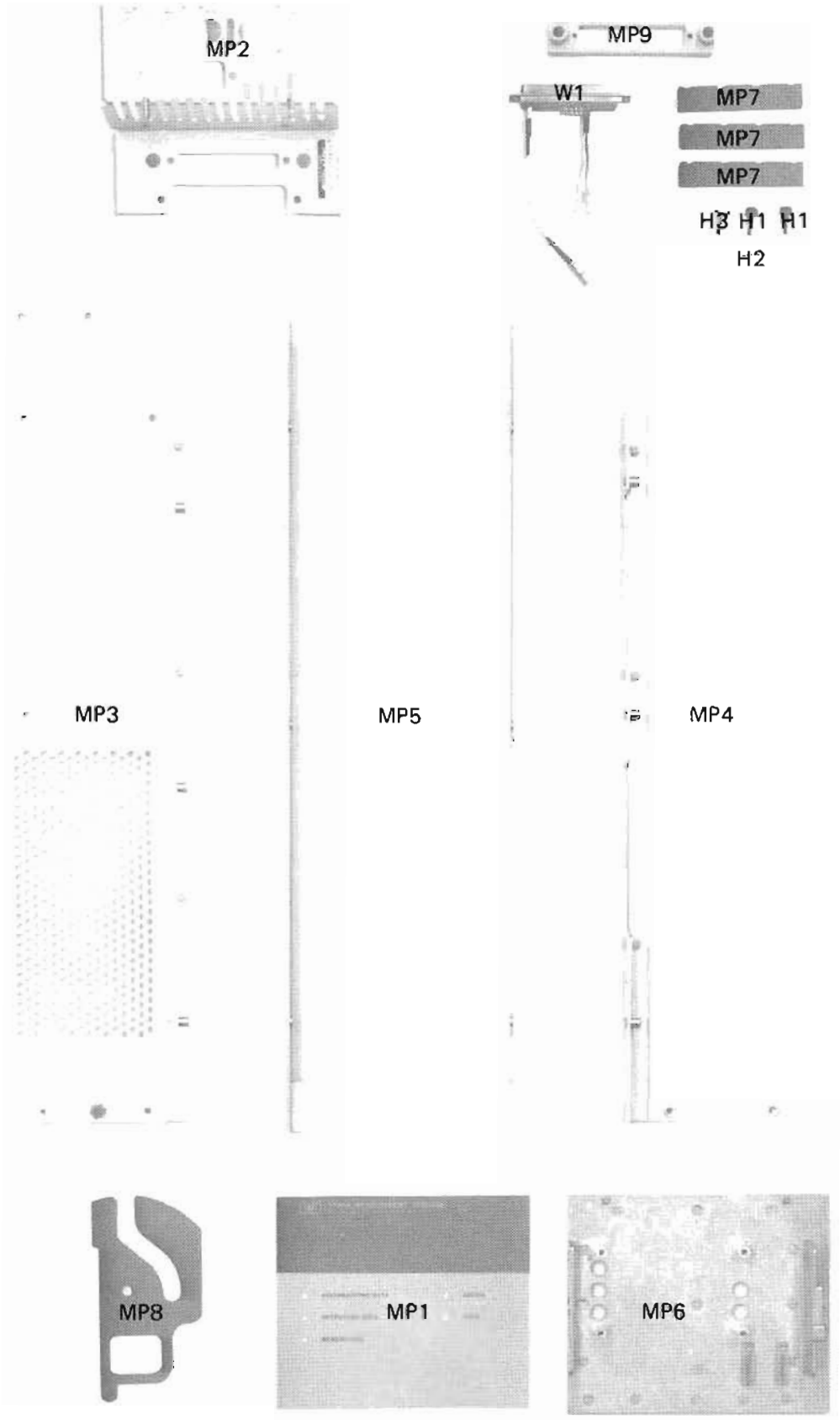


Figure 6-1. 5358A Cabinet Parts

SECTION VII
MANUAL CHANGES

7-1. INTRODUCTION

7-2. This section contains information necessary to adapt this manual to apply to newer instruments.

7-3. MANUAL CHANGES

7-4. This manual applies directly to Model 5358A Measurement Storage Plug-Ins with prefix 1628A, 1640A. As engineering changes are made, newer instruments may have serial prefix numbers higher than those listed on the title page of this manual. The manuals for these instruments will be supplied with "MANUAL CHANGES" sheets containing the required information. Replace affected pages or modify existing manual information as directed in the "MANUAL CHANGES" pages. Contact the nearest Hewlett-Packard Sales and Service Office if the change information is missing.

SECTION VIII
SERVICE

8–1. INTRODUCTION

8–2. This section contains assembly designations, signal mnemonics, identification marking descriptions, theory of operation, diagnostics general descriptions, troubleshooting, schematic diagrams, and part locators. The part locators show the location by reference designator.

8–3. SCHEMATIC DIAGRAM SYMBOLS AND REFERENCE DESIGNATORS

8–4. *Figure 8–1* shows the symbols used on the schematic diagrams. At the bottom of *Figure 8–1*, the system for reference designators, assemblies, and subassemblies is shown.

8–5. ASSEMBLY DESIGNATIONS

8–6. *Table 8–1* lists the designations, name, and HP Part Number of assemblies used in the 5358A.

8–7. Reference Designations

8–8. Assemblies such as printed-circuit boards are assigned numbers in sequence, A1, A2, etc. As shown in *Figure 8–1*, subassemblies within an assembly are given a subordinate A number. For example, rectifier subassembly A1 has the complete designator of A25A1. For individual components, the complete designator is determined by adding the assembly number and subassembly number, if any. For example, CR1 on the rectifier assembly is designated A25A1CR1.

8–8. SIGNAL MNEMONICS

8–10. *Table 8–2* contains a list of the mnemonics used to identify signals on the schematic diagrams.

8–11. IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS

8–12. HP printed-circuit boards (see *Figure 8–1*) have four identification numbers; an assembly part number, a series number, a revision letter, and a production code.

Table 8–1. Assembly Identification

ASSEMBLY	DESCRIPTION	HP PART NO.
A1	HP-IB Input	05358–60001
A2	Motherboard	05358–60002
A3	HP-IB Control	05358–60003
A4	Memory Control	05358–60004
A5	System Control	05358–60005
A6	Gate Control	05358–60006
A7	Converter	05358–60007
A8	Memory	05358–60008
A9, A10, A11	Memory (Optional)	05358–60008
A12	Display	05358–60009
A13	BNC I/O	05358–60010

SYMBOLS

FRONT PANEL

REAR PANEL

INTERIOR AND PC BOARDS

WIPER MOVES TOWARD "CW" WHEN CONTROL IS ROTATED CLOCKWISE

POWER LINE GROUND

CIRCUIT COMMON GROUND

FLOATING GROUND

CHASSIS GROUND

KNOB CONTROL

SCREWDRIVER ADJUST

MAIN SIGNAL PATH

FEEDBACK PATH

TEST POINT

"AND" GATE

"OR" GATE

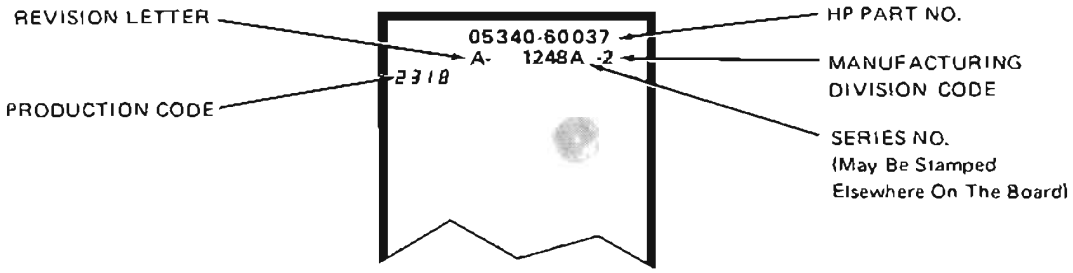
INVERTER

NAND GATE

NOR GATE

EXCLUSIVE NOR

PRINTED CIRCUIT BOARD IDENTIFICATION



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

ASSEMBLY	ABBREVIATION	COMPLETE DESCRIPTION
A25	C1	A15C1
A25A1	CR1	A25A1CR1
NO PREFIX	J3	J3

2. UNLESS OTHERWISE INDICATED.
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES.
3. JACKS ARE THE STATIONARY CONNECTORS AND PLUGS ARE THE MORE MOVEABLE OF TWO CONNECTORS.

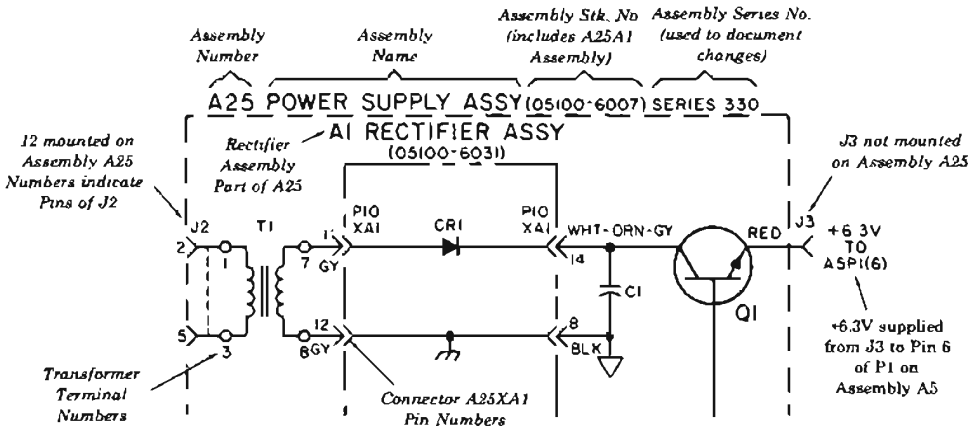


Figure 8-1. Schematic Diagram Notes

Table 8-2. Signal Descriptions, Source, and Destinations

ABBREVIATIONS	CONNECTOR & PINS		DESCRIPTION
	FROM	TO	
$\overline{\text{ACCUM}}$	A5P1($\overline{21}$)	A3P2B(1) A4P1A(21)	Signal from A5 System Control to A4 Memory Control and A3 HP-IB to indicate 5358A is in the accumulating mode.
ACCUM DATA	A5P1($\overline{20}$)	A2J3(8)	A5 System Control signal to front panel ACCUMULATING DATA indicator.
ACC CMD + GET	A3P2B(5)	A5P1(16) via A3P2A(16) & A4P1A(16)	Initiate (I) Program Code OR'ed with Group Execute Trigger (GET) on A3 HP-IB and sent to A5 System Control to initiate data transfer.
$\overline{\text{ACCUM HALT}}$	A3P2A(22)	A5P1($\overline{22}$)	Stop (H) Program Code from A3 HP-IB decoder to A5 System Control.
ACCUM TRIG IN	A2J1(10)	A5P1($\overline{1}$)	External Trigger via rear panel connector to A5 System Control.
ADDR CLR ADDR DN CLK ADDR UP CLK	—	—	A3 HP-IB Control signals to buffer address counter.
ADDR TRANS CLK	—	—	A4 Memory Control clock to address Multiplexers.
ADDR STOBE	—	—	A4 Memory Control strobe to Address Counter Reset selector.
ADDR R/W	—	—	A4 Memory Control word select to address multiplexers.
ADDR RD CLK	—	—	A4 Memory Control clock to Read Address counter.
ADDR WRT CLK	—	—	A4 Memory Control clock to Write Address counter.
ARMED	A2P1(13)	A6P1(18)	Signal from 5345A indicating it's armed (ready to take a measurment).
DELAY ACCUM	A5P1(9)	A6P1(9)	Inhibits error condition S2 from being activated if data is not being transferred.
	A4P1)B	A8,A9,A10,A11	Address lines from A4 Memory Control provide addressing to memory circuits on A8 Memory.
A1	(1)	(1)	
A2	(2)	(2)	
A3	(3)	(3)	
A4	(4)	(4)	
A5	(5)	(5)	
A6	(6)	(6)	
A7	(7)	(7)	
A8	(8)	(8)	
A9	(9)	(9)	
A10	(10)	(10)	
A11	(11)	(11)	
$\overline{\text{B1}}$	—	—	These bits are output on an internal bus that passes either the status Byte or the memory data from the A3 buffers. The internal bus provides an output to the HP-IB bus.
$\overline{\text{B2}}$	—	—	
$\overline{\text{B3}}$	—	—	
$\overline{\text{B4}}$	—	—	
$\overline{\text{B5}}$	—	—	
$\overline{\text{B6}}$	—	—	
$\overline{\text{B7}}$	—	—	
$\overline{\text{B8}}$	—	—	
$\frac{\text{C}}{\overline{\text{C}}}$	—	—	A3 HP-IB ASCII state machine format circuit output for "comma".

Table 8-2. Signal Descriptions, Source, and Destinations (Continued)

ABBREVIATIONS	CONNECTOR & PINS		DESCRIPTION
	FROM	TO	
$\overline{\text{CLR HOLD}}$ $\overline{\text{CLR HOLD}}$	— —	— —	A4 Memory Control Assembly control lines for Memory Clear cycle.
CR CR	— —	— —	A3 HP-IB ASCII state machine format circuit output for "carriage return".
DAV	A3P1A(9)	A1J1(6)	Handshake signal Data Valid between A3 HP-IB and HP-IB bus.
$\overline{\text{DEAD}}$	A6P1(5)	A2J1(4)	Low External Gate signal from A6 Gate Control to rear panel Sample Time $\overline{\text{DEAD}}$ connector. Provided for use with a second 5345A.
DEAD TIME START DEAD TIME STOP	A6(1($\overline{1}$) A2J1(6)	A2J1(12) A6P1(4)	Provide control of dead time by an external device via rear panel connectors.
DATA CLK 1	A5P1($\overline{11}$)	A4P1A(11)	A5 System Control data clock signal to A4 Memory Control to latch in the first of two digits from the 5345A.
	A4P1B	A8,A9,A10,A11	Data Input bits to A8 (A9, A10, A11) Memory from A4 Memory Control data drive circuits.
DI1	($\overline{1}$)	($\overline{1}$)	
DI2	($\overline{2}$)	($\overline{2}$)	
DI3	($\overline{3}$)	($\overline{3}$)	
DI4	($\overline{4}$)	($\overline{4}$)	
DI5	($\overline{5}$)	($\overline{5}$)	
DI6	($\overline{6}$)	($\overline{6}$)	
DI7	($\overline{7}$)	($\overline{7}$)	
DI8	($\overline{8}$)	($\overline{8}$)	
	A1J1	A3P1A	HP-IB data input/output bits between A3 HP-IB circuits and HP-IB bus.
DIO1	(1)	($\overline{10}$)	
DIO2	(2)	($\overline{11}$)	
DIO3	(3)	(12)	
DIO4	(4)	(8)	
DIO5	(13)	(9)	
DIO6	(14)	(11)	
DIO7	(15)	($\overline{7}$)	
DIO8	(16)	(8)	
DIR CLR	—	—	A6 Gate Control count chain clear signal to clear the Meas and Dead generation circuit.
	A8P1–A11P1	A3P2B	Data output bits from A8 (or A9, A10, A11) Memory to A3 HP-IB Buffer.
DO1	($\overline{9}$)	($\overline{9}$)	
DO2	($\overline{10}$)	($\overline{10}$)	
DO3	($\overline{11}$)	($\overline{11}$)	
DO4	($\overline{12}$)	($\overline{12}$)	
DO5	($\overline{13}$)	($\overline{13}$)	
DO6	($\overline{14}$)	($\overline{14}$)	
DO7	($\overline{15}$)	($\overline{15}$)	
DO8	($\overline{16}$)	($\overline{16}$)	
DRA DRB DRC DRD	A2P1(1) A2P1(4) A2P1(2) A2P1(3)	A4P1B(4) A4P1B(5) A4P1B(6) A4P1B(9)	Data from 5345A to data circuit on A4 Memory Control.
E/F CLK and DATA CLK 3	—	—	A4 Memory Control clock from Memory Request Logic to Empty/Full Up/Down counts and Data Input Driver.
$\overline{\text{EMPTY}}$	A4P1B($\overline{12}$)	A3P2B(3)	A4 Memory Control low signal from Empty/Full circuit to A3 HP-IB, indicating memory is empty.

Table 8-2. Signal Descriptions, Source, and Destinations (Continued)

ABBREVIATIONS	CONNECTOR & PINS		DESCRIPTION
	FROM	TO	
E/F U/$\overline{D}$	—	—	A4 Memory Control signal from Memory Request Logic to Empty/ Full Up/Down counters.
$\overline{\text{FREE RUN}}$	A1J2(7)	A5P1(17), via A2P1A(3), A3P2A(17), A4P1A(17)	Signal from rear panel FREE RUN switch (marked X) that sets 5358A in full-run mode.
FULL	A4P1B(20)	A2J3(4),A5P1($\overline{14}$), A3P2B($\overline{1}$) via A4P1A(14) and A3P2A($\overline{14}$)	A4 Memory Control signal from Empty/Full circuit to A3 HP-IB, A5 System Control and front panel indicator.
EXT DT IN	—	—	Signal on A6 Gate Control from Dead Time Stop circuit to End Ext Dead Time FF.
F1 F2 F3 F4	A8P1(17) A9P1(17) A10P1(17) A11P1(17)	A4P1B(17) A4P1B(18) A4P1B(19) A4P1B(20)	Lines from memory boards to Memory Control decoders indicate the number of memory boards installed in the plug-in.
EDTSL IN	—	—	Signal on A6 Gate Control to invert the sense of the External Dead Time In signal.
EDTSL OUT	—	—	Signal on A6 Gate Control to invert the sense of the External Dead Time Out signal.
$\overline{\text{HOLD BOTH}}$	—	—	When low to A6Q6, causes $\overline{\text{MEAS}}$ and $\overline{\text{DEAD}}$ to hold to ground level.
$\overline{\text{INH PROC}}$	A5P1(13)	A2P1(15)	A5 System Control signal to 5345A that inhibits the processing cycle when memory is full.
$\overline{K}$	A3P2A($\overline{13}$)	A6P1A(14) via A4P1A($\overline{13}$)	Gate Generator reset program code (K) from A3 HP-IB decoder that clears the A6 System Control.
LISTEN	A3P2B(19)	J3(12)	A3 HP-IB Listen FF signal to front panel LISTEN indicator.
LOAD/UNLOAD	—	—	A3 HP-IB signals from Load FF indicate when formatter is in loading or unloading mode.
LF $\overline{\text{LF}}$	—	—	A3 HP-IB ASCII state machine format circuit output for "linefeed".
$\overline{\text{MEAS}}$	A6P1(13)	A2J1(2)	Low External Gate signal for 5345A from A6 Gate Control to rear panel SAMPLE TIME $\overline{\text{MEAS}}$ connector.
MEAS TIME	A2P1(42)	A5P1(21)	5345A signal to indicate period of time when mainframe is taking a measurement.
MEM CLR	A3P2B(7)	A4P1A(7),A5P1(7), via A3P2A(7)	Memory clear signal from A3 HP-IB to A4 Memory Control and A5 System Control.
MEM WRT CLK	A3P2B(12)	A4P1A($\overline{12}$)	Clock signal from A3 HP-IB to A4 Memory Control Write Request circuit.
$\overline{\text{M CLK HOLD}}$	—	—	A6 Gate Control signal inhibits the Master Clock to the counter chain.
MF DATA CLK	A5P1($\overline{9}$)	A4P1A($\overline{9}$)	Clock signal from A5 System Control to Memory Request Logic and Data Latch circuit on A4 Memory Control.

Table 8-2. Signal Descriptions, Source, and Destinations (Continued)

ABBREVIATIONS	CONNECTOR & PINS		DESCRIPTION
	FROM	TO	
$\overline{\text{MIN DT}}$	—	—	A6 Gate Control signal from Dead Time Selector to Meas and Dead Generation circuit for minimum Dead Time mode.
MOD DECADE OUT	—	—	A6 Gate Control Modified Decade output signal to MEAS and DEAD circuits.
MS1	A4P1B(13)	A8P1(13)	MS1, 2, 3, and 4 are module select signals that activate memory boards A8, A9, A10, and A11, respectively. (A9, A10, A11 are optional.) Signals are sent from A4 Memory Control to Memory boards.
MS2	A4P1B(14)	A9P1(13) via A8P1(14), A9P1(14)	
MS3	A4P1B(15)	A10P1(13) via A8P1(15), A9P1(15), A10P1(15)	
MS5	A4P1B(16)	A11P1(13) via A8P1(16), A9P1(16), A10P1(16), A11P1(16)	
M•BCD	—	—	Unloading mode for BCD.
M•BIN	—	—	Unloading mode for binary.
$\overline{\text{NRC—Ø}}$	A5P1(7)	W5J1(1) via A2	"Numerator Register (NR Counter) goes to Ø" signal from A5 System Control to 5345A.
NDAC	A3P1A(10)	A1P1(8)	Handshake signals Not Data Accepted and Not Ready for Data between A3 HP-IB and HP-IB bus.
NRFD	A3P1A($\overline{12}$)	A1P1(7)	
OUTPUTTING DATA	A3P2B(20)	A2J3(6)	A3 HP-IB signal from formatter circuit to front panel OUTPUTTING DATA indicator.
	A3P2A	A4P1A,A5P1,A6P1	Programmed Data Bits from A3 HP-IB to A4 Data circuit, to A5 System Control and to A6 Gate Control.
PDBØ	($\overline{15}$)	($\overline{15}$)	
PDB1	($\overline{16}$)	($\overline{16}$)	
PDB2	($\overline{17}$)	($\overline{17}$)	
PDB3	($\overline{18}$)	($\overline{18}$)	
PDB4	A3P2A($\overline{19}$)	A4P1A($\overline{19}$)	Programmed Data Bits from A3 HP-IB to A4 Data circuit.
PDB5	A3P2A($\overline{20}$)	A4P1A($\overline{20}$)	
PDB6	A3P2A($\overline{21}$)	A4P1A($\overline{21}$)	
PDB7	A3P2A($\overline{22}$)	A4P1A($\overline{22}$)	
PI CLK	A2P1(16)	A5P1($\overline{10}$)	Data Transfer clock from 5345A to A5 System Control circuit that generates Data CLK 1 and MF Data CLK.
$\overline{\text{PI CLK EN}}$	A2P1(21)	A5P1($\overline{8}$)	Plug-in clock enable signal from 5345A to A5 System Control.
$\overline{\text{PI DUMP}}$	A2P1(5)	W5J1(2) via A2	Low signal from A5 System Control causes 5345A to transfer data to the 5358A.
$\overline{\text{PI INH ARM}}$	A5P1(12)	A2P1(40), A6P1(12)	Low signal from A5 System Control inhibits arming of 5345A and A6 Gate Control generation.
PRCD	A3P2A(21)	A6P1($\overline{13}$)	Signal from A3 HP-IB decoder to A6 Gate Control that clocks the D-register.

Table 8-2. Signal Descriptions, Source, and Destinations (Continued)

ABBREVIATIONS	CONNECTOR & PINS		DESCRIPTION
	FROM	TO	
PRCE	A3P2A(9)	A6P1($\overline{9}$)	Signal from A3 HP-IB decoder to A6 Gate Control that clocks the E-register.
PRCF	—	—	Signal on A3 HP-IB from decoder that clocks the F-register.
PRCM	A3P2A(18)	A6P1(19) via A4P1A(18), A5P1(19)	Signal from A3 HP-IB decoder to A6 Gate Control that clocks the M-register.
PRCN	A3P2A(19)	A5P1($\overline{13}$)	Signal from A3 HP-IB decoder that clocks numbers into A5 System Control N-register.
$\overline{\text{PRCS}}$	A3P2A(11)	A5P1(11)	Signal from A3 HP-IB decoder that clocks code numbers into A5 System Control G-register.
PRCT	—	—	Signal on A3 HP-IB from decoder to clock the T-register.
$\overline{\text{PRRM}}$	A3P2A(20)	A6P1($\overline{14}$)	Low signal from A3 HP-IB decoder to A6 Gate Control that clears the M-register.
$\overline{\text{PRRN}}$	A3P2A(9)	A5P1($\overline{12}$)	Low signal from A3 HP-IB decoder that resets A5 System Control N-register to all Ø's.
$\overline{\text{PRRT}}$	—	—	Low signal on A3 HP-IB resets the T-register to all Ø's.
$\overline{\text{PROC BUSY}}$	A2P1(32)	A5P1(18)	Low signal from 5345A indicates that a measurement has been completed and a processing cycle has started.
$\overline{\text{PWR DOWN}}$	A4P1A(1)	A3P2B(8)	Signal to indicate a Power-Down condition which could destroy data in memory.
$\overline{\text{PWR UP}}$	A4P1A(5)	A3P2B($\overline{6}$), A5P1(14), A6P1($\overline{7}$) via A3P2A($\overline{5}$)	Signal used for Powering Up logic circuits to a preset state.
RD ACCEPTED	A4P1($\overline{11}$)	A3P1B(11) via A3P2A(12)	Signal from A4 Memory Control to T-counter on A3 HP-IB. Clocks count-down to keep track of data sent to buffers.
RD REQUEST	A3P1B(13)	A4P1A($\overline{8}$) via A3P2A($\overline{8}$)	Signal from A3 HP-IB to A4 Memory Control that requests a Read Cycle.
$\overline{\text{RD STROBE}}$	A4P1A(12)	A3P1B(11) via A3P2A(12)	Signal from A4 Memory Control that allows data to be clocked into HP-IB buffers.
$\overline{\text{RST}}$	A2P1(38)	A5P1(22)	5345A reset signal to A5 System Control.
SPMS $\overline{\text{SPMS}}$	— —	— —	A3 HP-IB Serial Poll Mode FF signals to Handshake and Status circuits.
STATUS CLK	—	—	A4 Memory Control status clock from Memory Request Logic to Status FFs.
$\overline{\text{S2}}$	A6P1($\overline{5}$)	A3P2B(4) via A3P2A(1)	Status signal (Programmed Dead Time < True Dead Time) from A6 Gate Control to A3 HP-IB.

Table 8-2. Signal Descriptions, Source, and Destinations (Continued)

ABBREVIATIONS	CONNECTOR & PINS		DESCRIPTION
	FROM	TO	
$\overline{S3}$	A5P1(15)	A3P2B(6) via A3P2A(15), via A4P1A(15)	Status signal (Sync Error Due to Memory Full) from A5 System Control to A3 HP-IB.
S4	A4P1B($\overline{18}$)	A3P2B($\overline{3}$)	Memory Status signal code from A4 Memory Control to A3 HP-IB.
$\overline{S5}$	A4P1B($\overline{19}$)	A3P2B($\overline{2}$)	Memory Status signal code from A4 Memory Control to A3 HP-IB.
$\overline{S6}$	A5P1($\overline{19}$)	A3P2B(2)	Status signal (completed N measurements) from A5 System Control to A3 HP-IB.
SRQ	—	—	A3 HP-IB signal from SRQ (Service Request) Generator to HP-IB bus.
TALK	A3P2B(18)	A12J3(14) via A2J3(14)	A3 HP-IB Talk FF signal to front panel TALK indicator.
TACS	—	—	A3 HP-IB signal (TALKER ACTIVE STATE) from TALK circuit to OUTPUTTING DATA circuits.
TA	A3P2B(17)	A5P1($\overline{4}$) via A3P2A($\overline{4}$)	A3 HP-IB T-register output to HP-IB format T-counter and to A5 System Control T-counter to count number of digits transferred over from 5345A.
TB	A3P2B(15)	A5P1(6) via A3P2A(6)	
TC	A3P2B(14)	A5P1($\overline{6}$) via A3P2A($\overline{6}$)	
TD	A3P2B(16)	A5P1($\overline{5}$) via A5P2A(5), and A4P1A(20)	A3 HP-IB T-register output to HP-IB format T-counter and to A5 System Control T-counter to count number of digits transferred over from 5345A.
TE	A3P1B($\overline{19}$)	A5P1(10) via A4P1A(19)	
TC=Ø	—	—	A3 HP-IB Format "T-counter equal to zero" signal.
$\overline{WE}$	A4P1B($\overline{17}$)	A8—A11P1($\overline{17}$)	Write Enable from A4 Memory Control to A8 Memory circuits.
$\frac{T}{\overline{T}}$	—	—	A3 HP-IB ASCII formatter control signal to select one of two data buffers for outputting onto HP-IB.
$\overline{WRT\ DATA\ CLK}$	—	—	A4 Memory Control clock signal that clocks Data Latch circuit on receipt of a WRT DATA request.
1/4V	A1J2(6)	A5P1(4) via A3P1A($\overline{3}$)	Signal from rear panel switch marked Y for 1-volt or 4-volt ACCUM TRIG INPUT signal.
1 MHz CLK	A4P1A(14)	A3P2A(14) A6P1(16)	Clock signal from A4 Memory Control to A3 HP-IB Handshake circuit and A6 Gate Control reset circuit.
5 MHz CLK	A4P1A(13)	A3P2A(13)	Clock signal from A4 Memory Control to A3 HP-IB Listen, Talk, and SPM FFs.
10 MHz CLK	A4P1A($\overline{6}$)	A6P1($\overline{6}$)	Clock signal generated by A4 Memory Control to clock A6 Gate Control count chain.
10 MHz 10 MHz RET	A2J2(center) A2J2(shield)	A4P1A($\overline{4}$) A4P1A($\overline{7}$)	Signal from 5345A counter to A4 Memory Control.

8–13. The assembly part number has 10 digits (such as 05358–60001) and is the primary identification. All assemblies with the same part number are interchangeable. When a production change is made on an assembly that makes it incompatible with previous assemblies, a change in part number is required. The series number (such as 1624) is used to document minor electrical changes. As changes are made, the series number is incremented. When replacement boards are ordered, you may receive a replacement with a different series number. If there is a difference between the series number marked on the board and the schematic in this manual, a minor electrical difference exists. If the number on the printed-circuit board is lower than that on the schematic, refer to Section VII for backdating information. If it is higher, refer to the loose-leaf manual change sheets for this manual. If the manual change sheets are missing, contact your local Hewlett-Packard Sales and Service Office. See the listing on the back cover of this manual.

8–14. Revision letters (A, B, etc.) denote changes in printed-circuit layout. For example, if a capacitor type is changed (electrical value may remain the same) and requires different spacing for its leads, the printed-circuit board layout is changed and the revision letter is incremented to the next letter. When a revision letter changes, the series number is also usually changed. The production code is the four-digit, seven-segment number used for production purposes.

8–15. Symbols are used on PC boards to aid in identifying pin number, diode elements, etc., as follows:

Δ OR □

IDENTIFIES:

Pin 1 of dip and flat-pack IC's.
Tab of TO cases.
+ side of electrolytic capacitors.
Pin 1 of resistor packs.
Cathode of diodes.
Section 1 of dip switches.

8–16. ASSEMBLY LOCATIONS AND COMPONENT LOCATORS

8–17. *Figures 8–3, 8–4,* and *8–5* show the front, rear, and top view of the 5358A, respectively. The front and rear views show reference designators of the front and rear panel controls, connectors, and indicators. The top view shows assembly locations. Component locators for each printed-circuit assembly are located next to the schematics.

8–18. THEORY OF OPERATION

8–19. Paragraphs 8–20 through 8–37 explain the block theory of operation of each of the active boards according to the block diagram in *Figure 8–2.* A detailed circuit theory immediately follows the block theory in paragraph 8–38 through 8–115

8–20. A3 HP-IB Control Assembly

8–21. As shown in the block diagram, *Figure 8–2,* the HP-IB bus lines are connected through the A1 HP-IB connector board to A3 HP-IB assembly to provide an interface between other HP-IB units and the 5358A. Information and program codes from the bus are received by the A3 address and decoder circuits and are passed to other 5358A circuits. The data from A8 memory is sent out to the bus through the A3 buffers and controlled by the format circuits. The service request and status byte circuits are also contained on A3.

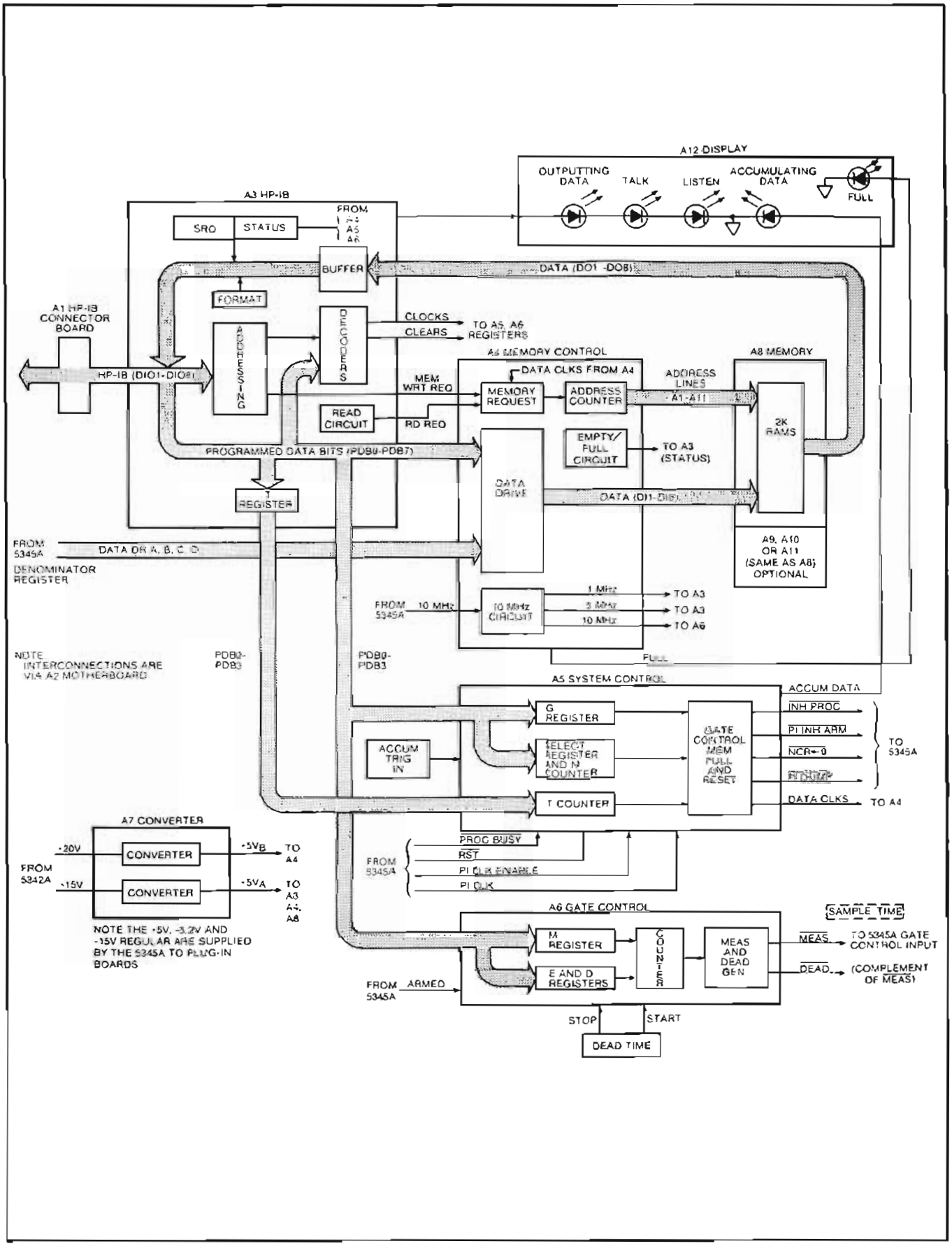


Figure 8-2. 5358A Block Diagram

8–22. The programmed data bits PDB0—PDB7 are sent via A3 to the data drive circuits of A4 Memory Control. Bits 0—3 are sent as program codes to the register that control the operation of A5 System Control and A6 Gate Control.

8–23. A4 Memory Control Assembly

8–24. A4 Memory Control circuits control the operation of A8 Memory and provide power-up, power-down and clock generation circuits. The memory request logic has an I/O sequencer that controls the read, write, and clear cycles which are initiated by A3 HP-IB and A5 System Control signals. The address counter generates addressing for A8 Memory. The data drive circuit selects data from A3 HP-IB or from the 5345A denominator register (DRA, B, C, D).

8–25. The A4 clock generation circuit receives 10 MHz from the 5345A and sends a 1 MHz and a 5 MHz clock to A3 and a 10 MHz clock to A6. The empty/full status of memory is provided by A4 to the status circuits on A3 HP-IB.

8–26. A5 System Control Assembly

8–27. The A5 System Control controls the processing of data from the 5345A by A4 Memory Control. The $\overline{\text{PI DUMP}}$ signal from A5 causes the 5345A to transfer data to the 5358A. The $\overline{\text{PROC BUSY}}$ signal from the 5345A stays active low during the transfer of data.

8–28. The G-register on A5 receives a trigger from A3 (or from a rear panel input) to start a measurement. The G-register is programmed by program codes on the bus for continuous (not counted) mode or N measurement (counted) mode. The N-register receives code N followed by one to four digits to control the number of measurement. The T-counter receives inputs from A3 and controls the number of digits transferred from the 5345A. The $\overline{\text{PI INH ARM}}$ results from a program code and acts to inhibit arming of the 5345A and also synchronizes the A6 circuits to hold $\overline{\text{MEAS}}$.

8–29. The $\overline{\text{ACCUM}}$ signal goes to the front panel indicator and to S3 and A4 to indicate the 5358A is accumulating data from the 5345A and to stop accepting data from the bus. Status signals are sent from A5 to A3.

8–30. A6 Gate Control Assembly

8–31. A6 Gate Control circuit controls the time period of the measurement taken by the 5345A. The measurement time and the ratio of measurement/dead time are controlled by program codes to the M (mantissa), E (exponent), and D (dead time) registers. The dead time can also be controlled by an external device connected via rear panel BNC connectors STOP and START. The $\overline{\text{MEAS}}$ signal from A6 goes to the 5345A GATE CONTROL INPUT rear panel BNC connector and controls the measurement time period.

8–32. A7 Converter Assembly

8–33. A7 Converter receives +20V and +15V from the 5345A and converts these voltages to $+5V_B$ for A4 and $+5V_A$ for A3, A4 and A8. The +5V, -5.2V and -15V regular operating voltages used by the 5358A circuits are received from the 5345A.

8–34. A8 Memory Assembly

8–35. A8 Memory contains 16 RAM's divided into two groups of eight (1K) for a total memory of 2K (each RAM has 1024 cells and stores one bit in each cell). Each of the data-in lines (DI1—DI8) and each of the data-out lines (DO1—DO8) is connected to one of the RAM's in each group. The addressing and control lines and data inputs come from A4 Memory Control. Up to three additional memory assemblies (A9, A10, A11) may be installed for a total memory of 8K.

8-36. A12 Display Assembly

8-37. A12 Display provides the front panel indicators that are activated by signals from A3 HP-IB (OUTPUTTING DATA, TALK, and LISTEN), from A5 System Control (ACCUMULATING DATA) and from A4 Memory Control for indicating memory FULL.

8-38. DETAILED CIRCUIT THEORY

8-39. A1 HP-IB Input

8-40. The A1 HP-IB Input is a connector board that connects the HP-IB bus to the A3 HP-IB assembly. The address switch S1 is mounted on A1. (See *Figure 8-7*, sheet 1.)

8-41. A2 Motherboard

8-42. The A2 Motherboard provides interconnections between the plug-in boards of the 5358A. Connectors for the board are mounted on A2.

8-43. A3 HP-IB

8-44. The A3 HP-IB assembly acts as an interface between the HP-IB bus and the 5358A circuits. The HP-IB bus information and program codes are received and processed by the A3 circuits. The data from memory and status information for the 5358A are sent to the bus through A3.

8-45. The A3 HP-IB circuits are shown in *Figure 8-7*, Sheets 1 through 4.

8-46. SHEET 1, *FIGURE 8-7*. Sheet 1 contains Input/Output Addressing, Decoding, and Handshake circuits.

8-47. The bus is connected through A1 HP-IB Input (connector board) to A3 HP-IB assembly. The address switch (S1) is also connected to the input lines through comparator A3U1. When the logic state of the bus DIO lines compares with that of address switch settings A2—A5, the comparator activates either Talk FF U16A or Listen FF U16B (through U14A), depending upon the state of DIO lines 6 and 7. The A1 portion of the address switch is not connected because the bit on the DIO1 line is detected by the address or decoding circuits as either bus information or a programming code. The A6 portion of the address switch is connected to the External Trigger circuit on A5 System Control to set the trigger level to 1 (50Ω load) or 4 (TTL load) volts. The A7 portion of the Address Switch provides a FREE RUN position to place the 5358A in the "talk always" mode.

8-48. The Device Clear or Selected Device Clear commands on the bus are detected by U25 and Group Execute Trigger (GET) or Serial Poll Enable or Disable are detected by U14B.

8-49. The program codes are decoded by U21, U23, and U24. Program codes detected by U21 result in clock signals PRCM, PRCD, and PRCE to the M, D, and E registers, respectively, on the A6 Gate Control assembly. Clock signal $\overline{\text{PRCS}}$ is sent to the G-register and PRCN to the N-register on A5 System Control. Clock signal PRCT goes to the T-register on the HP-IB assembly. The functions of the registers are described under their circuit descriptions that follow.

8-50. Signals to clear the registers (when required) are sent by U24 in addition to the K clear to A6 Gate Control assembly and $\overline{\text{ACCUM HALT}}$ to A5 System Control.

8-51. The programmed data bit lines PDBØ THROUGH PDB7 provide 8 lines for memory data through A4 Memory Control to the A8 (A9, A10, or A11 optional) memory assembly (used for

diagnostic data). If a programming code is being sent, only the lower four-bit lines (PDBØ-PBD3) are used. These four lines go the T-register of A3, to the Data Drive circuit of A4, to the G-register of A5 and to the M-register of A6.

8-52. The circuits associated with FFs U12A and B develop the Listen Handshake for the HP-IB bus. Inputs to this circuit are the 1 MHz clock from A4 Memory Control, the $\overline{\text{ACCUM}}$ signal from A5 System Control and the Full signal from A4 Memory Control.

8-53. SHEET 2, *FIGURE 8-7*. Sheet 2 contains the Status Latch, SRQ Request, SRQ Generation, Source Handshake, and Status Byte circuits.

8-54. Status Latch U33 receives status $\overline{\text{S2}}$ (programmed dead time < actual dead time) from A6 Gate Control, $\overline{\text{S3}}$ (sync error due to memory full) and $\overline{\text{S6}}$ (completed N measurements) from A5 System Control in addition to $\overline{\text{PWR DOWN}}$ from A4 Memory Control.

8-55. The Source Handshake circuit U40A and B and associated gates control the bus handshake for the talk output.

8-56. A service request condition such as power down will cause the SRQ request and SRQ generation circuit to output the SRQ OUT signal to indicate to the controller that service is requested. The controller requests status by serial poll which is detected by the SPM FF U17A Sheet 1). The $\overline{\text{SPMS}}$ signal causes the Status Byte circuit to output the status to the bus. Status is indicated by the state (1 or Ø) of the $\overline{\text{B1}}$—$\overline{\text{B8}}$ bits in the status byte as follows:

$\overline{\text{B1}}$ — Power Down
$\overline{\text{B2}}$ — Programmed dead time < true dead time
$\overline{\text{B3}}$ — Sync error due to Memory Full.
$\overline{\text{B4}}$ — Memory 00 Empty
$\overline{\text{B5}}$ — Full 01 <1/2 Full
10 ≥1/2 Full
11 Full
$\overline{\text{B6}}$ — N measurements complete
$\overline{\text{B7}}$ — Service Request
$\overline{\text{B8}}$ — Not assigned.

3-57. For example, if $\overline{\text{B1}}$ (power down) is a "1", a power failure is indicated. This means that a power failure occurred after the last status readout. After status is read out the Status Byte circuit is cleared so a second request from the controller is required to obtain a new readout to determine if the condition is current.

8-58. SHEETS 3 AND 4, *FIGURE 8-7*. Sheets 3 and 4 consist of memory data circuits only. The purpose of these circuits is to take data from Memory, store it in a buffer and output the data to the output data bus.

8-59. The Read circuit (shown on Sheet 3) sends Read Request to A4 Memory Control which transmits it to A8 Memory to start the Read cycle. The memory board will shift 8 lines of data out to the data buffers (U46 and U48, Sheet 4) from where it is output to the bus when requested. A4 Memory Control sends the READ STROBE (a window of ≈40 μs) via U56B (Sheet 3) to the buffers for read-in.

8-60. The T-register (Sheet 3) outputs through the T-counter to the Format State Latch (Sheet 4) and to A5 System Control T-counter to count the number of digits transferred over from the 5345A.

8-61. The T-counter counts down with every read accept from A4 memory control, to keep track of how much data is sent out.

8–62. The F and T-register circuits are used to provide output formats in ASCII, Binary, MSD (first) or Binary, LSD (first).

8–63. The Address Clear and clock circuits (Sheet 3) control the Data Out Buffers (Sheet 4) through address counter U44 which is an up/down counter. The counter indicates when the address is Ø, used for determining memory empty.

8–64. The Format State Latch (Sheet 4) operates as a small state machine that does ASCII formatting by inserting the comma (C), carriage return (CR), and linefeed (LF), and keeps track of which digit is sent out.

8–65. In the ASCII format mode, the 8-bit byte of memory data is divided into two 4-bit BCD digits. The 4-bit BCD digits are then converted to 7-bit ASCII digits. The time digits are first sent followed by an ASCII comma (C) and then the events digits which are followed by a carriage return (CR), and a linefeed (LF). This sequence is alternated back and forth by the state machine which keeps track of which byte is being sent. In the case of the Binary format, both buffers are allowed to transfer data out to the data bus. The internal output bus (B1—B8 lines) is a three-state bus which passes status byte information or memory data information to the HP-IB bus. In addition, the internal bus is fed by the circuits that generate the Comma (C), Carriage Return (CR), or Linefeed (LF).

8–66. A4 Memory Control

8–67. The Memory Control assembly contains circuits for control of A8 Memory assembly in addition to Power-Up, Power-Down, and Clock Generation circuits.

8–68. The Memory Request Logic circuit shown in Sheet 1, *Figure 8–8*, contains shift register U7 that acts as an I/O sequencer to control the read and write processing circuits shown on Sheet 2, i.e., the Address Counter and Driver, Data Drive, and Empty/Full circuits. The sequencer generates control signals through latches U14A, B, C, and D to ensure proper timing of operation for the Read, Write, and Clear cycles. The cycles are initiated by signals from A3 HP-IB and A5 System Control.

8–69. The Data Drive circuit U15, U16, U17, U18, and U19 (Sheet 2) receives data from A3 HP-IB (IB1—IB8) and from the 5345A (LSD first) via A2 Motherboard A2P1 (DRA, B, C, D) and sends the data to the A8 Memory (A9, A10, and A11 optional).

8–70. Addressing is generated by the Address Counter and Driver circuit. The Write Address Counter U23, U29 lines are selected by multiplexers U21, U24, U27, and U30. The 13 lines from each address counter are combined in the multiplexers and sent through Drivers U22 and U25 for the A1—A11 address lines and $\overline{\text{WRITE ENABLE}}$ ($\overline{\text{WE}}$) to A8 Memory (A9, A10, and A11 optional). One output of U27 goes to U31 to generate the Module Select lines (MS1—MS4) for selection of the appropriate Memory assembly (if options installed).

8–71. The Empty/Full circuit uses Up/Down Counters U41, U42, U44, and U45 which are incremented in the Write mode and decremented in the Read mode. The F1, F2, F3, and F4 lines to Decoder U37 from A8, A9, A10, and A11 Memory assemblies, respectively, (A9, A10, and A11 optional) indicate to the Empty/Full circuit 2K, 4K, 6K, or 8K memory is installed. Memory Empty is detected by the up/down counters and sent through gate U34D and U36 as status. In addition to Empty and Full, status is required for less than 1/2 full and greater than or equal to 1/2 full. These status signals are provided by the Q outputs of the up/down counters through gate U43, multiplexer U35, and D-type FFs in U36. The logic states of status lines S4 and $\overline{\text{S5}}$ from U36 indicate Empty, Full, >1/2 full or ≤1/2 full. The input lines to multiplexer U35 pins 3, 4, 5, and 6 indicate "1/2 Full" and to pins 10, 11, 12, and 13 indicate "Full" for 2K, 4K, 6K, and 8K memory. The inputs are selected by U35 for output to D-type FFs in U36 which sends the memory status signals to A3 HP-IB for output to the Bus.

8–72. The clock generator circuits (Sheet 1) receives the 10 MHz sine wave signal from the 5345A via A2 Motherboard W5J1 and converts it through transisitors Q4, Q5, gate U1C and counter U2 to 1, 5 and 10 MHz square wave clock signals. The 1 MHz clock is sent to A3 HP-IB Listen, Talk, and SPM FFs. The 10 MHz clock is sent to A6 Gate Control M-counter.

8–73. The +5V input to A4 is monitored by the power-down circuit (Sheet 1). When the +5V drops below approximately 4V, the power-down circuit will sense the drop and send PRW DOWN to the Status Latch (U33) on the A3 HP-IB, which will result in a Service Request. When status is checked, power-down will be indicated.

8–74. A5 System Control

8–75. The A5 System Control board controls the processing of data by the 5358A. The data from the 5345A is sent to A8 Memory through A4 Memory Control but processing the data is controlled by A5 System Control. The A5 board receives the PI CLK EN and the PI CLK signals at U9 from the 5345A and generates the DATA CLK 1 and Mainframe DATA CLK for the Memory Control board.

8–76. A measurement is started by bus command I (initiate) or GET (Group Execute Trigger). These lines are OR'ed on the HP-IB board and sent to the System Control as ACCUM CMD +GET. An alternate method of triggering is provided by an external source via the external trigger rear panel connector to supply the ACCUM TRIG IN signal to A5. G-register U20 can be programmed to trigger on either the rising (G6 Code) or falling (G7 Code) edge. The X part of the rear panel address switch provides the FREE RUN signal via A3 HP-IB and the Y part provides the trigger level (1V 50Ω load or 4V TTL load) input to the External Trigger circuit.

8–77. The PI DUMP signal from the A5 board causes the 5345A to transfer data to the 5358A. The "Numerator Register Counter goes to 0" (NRC—0) signal resets the 5345A counter (numerator register) to ensure a clear display. The PROC BUSY signal from the 5345A indicates a measurement has been completed and the processing cycle is started. This signal stays active low during the transfer of data.

8–78. The G-register (U20) is controlled by codes of the program code set and can be programmed for continuous mode (G0) or for counted mode (G1). Stop codes are Halt (H), Memory Clear (DCL, SCL, R) or mainframe reset. Program code G4 is internal trigger and G5 is external trigger enable.

8–79. The N-register receives the code "N" followed by one, two, three, or four digits. The N-register consists of U16, U19, and U22, and the N counter is U15, U18, U21, and U23. The register sends data to the BCD counters. The PRRN signal resets the N-register to all 0's. Then, with the first number, the PRCN pulse occurs to clock in the number. The LSD counter is U15. When the N down-count gets to 0, the N Measurements Complete (N END) signal is sent out and does an internal Halt.

8–80. The T-Counter (U8 and U5) receives inputs from A3 HP-IB T-Register U43 and has an output range of 1—16. U8 outputs the LSD and U5 outputs 0 or 1 to control the number of digits transferred from the 5345A to the 5358A. U9 sends DATA CLOCK 1 to A4 Memory Control Data Drive circuit and MF DATA CLK to Memory Request Logic.

8–81. The G-register (U20) outputs PI HOLD or PI HOLD from program code G2 or G3, respectively. The PI HOLD and PROC BUSY signal (when not accumulating data) activate PI INH ARM which is sent via A2 Motherboard to the 5345A to inhibit arming. This signal also goes to the A6 Gate Control Board to hold the MEAS (gate) signal to synchronize the A6 circuits with the 5345A. When power is applied to the 5358A, the G-Register is automatically set to the following codes: 0, 2, 4, 6. These codes result in continuous mode (0), PI HOLD (2), External Trigger (4), and Falling Edge (6).

8–82. The $\overline{\text{INH PROC}}$ signal is sent to the 5345A from gate A5U11A to inhibit the processing cycle when memory is full. The ACCUM DATA signal from A5U14D goes to the front panel indicator ACCUMULATING DATA. The $\overline{\text{ACCUM}}$ signal from A5U14C indicates to A4 Memory Control Data Drive circuit that the 5358A is accumulating data and indicates to the A3 HP-IB to stop accepting data from the bus. The status signals $\overline{\text{S3}}$ (sync error due to memory full) and $\overline{\text{S6}}$ (completed N measurements) are sent to A3 HP-IB Status Latch U33. The DELAY ACCUM signal is sent from A5U11B to A6U6C to inhibit status signal $\overline{\text{S2}}$ (programmed dead time < actual dead time) if data is not being transferred.

8–83. A6 Gate Control

8–84. The A6 Gate Control circuits control the time period of the measurement taken by the 5345A. The 5345A indicates it is ready to take a measurement by sending the Armed signal via A2 Motherboard to gate A6U8B shown in *Figure 8–10*, Sheet 2, in the MEAS and Dead Generation circuit. The $\overline{\text{MEAS}}$ signal is then output from A6Q3 via a rear panel BNC connector to the 5345A GATE CONTROL INPUT. After a measurement is taken, the cycle repeats. The time period of the measurement is controlled by the program code sent to the Mantissa (M) and Exponent (E) registers shown in Sheet 1 of *Figure 8–10*.

8–85. The time period control circuits function to control the time of the measurement window and the nonmeasurement window, or the ratio of Meas/Dead time. A long gate time is used for close-in and a short gate time is used for farther out offset frequencies. (If a series of measurements were taken in the 5390A Sysstem and the information in the Times scaler of the 5345A did not change, then the phase noise would be zero.)

8–86. The measurement time (gate window) and the ratio Meas/Dead time are controlled by program codes to the registers shown in *Figure 8–10*, Sheet 1. The gate window can be varied from 1 μs to 999E7 (999×10^7) μ or 9990 seconds. Measurement time is programmed by an M (mantissa) code followed by 3 digits and an E (exponent) code followed by one-digit, for example:

M1EØ = 1 μ
MØØ1EØ = 1 μs

8–87. These codes are sent on lines PDBØ—PDB3 to Mantissa Register U20, U23, and to Exponent Register U15. The Mantissa Counter is made up of U19, U22, and U26 and the Exponent Counter (decade) is U14.

8–88. The Dead time register U17 with decoder U16 form the Dead time Selector. The Meas/Dead rates can be programmed as follows:

RATIO	PROGRAM CODE
Mainimum	DØK
1:1	D2K
2:1	D1K
External (External source such as HP 59309A Timing Generator)	D3K

8–89. With external dead time, the rear panel BNC connectors START and STOP are used for an external device to control the dead time and only the measurement time is programmed.

8–90. The $\overline{\text{MEAS}}$ and $\overline{\text{DEAD}}$ (complement of $\overline{\text{MEAS}}$) signals are sent to the rear panel BNC connectors. (The $\overline{\text{DEAD}}$ signal can be used to control a second 5345A.)

8–91. The 10 MHz clock signal from A4 Memory Control is received by the Count Pulse circuit at U18 (sheet 1). The Count Pulse is sent through the divide-by-5 circuit of U10 to the

Mantissa Counter which is a BCD counter with U19 the least significant digit (LSD). As the clock signal occurs, the counter counts as a cascading counter. The $\overline{\text{M CLK HOLD}}$ signal to U18 from U9A (Sheet 2) stops the count.

8-92. When Meas/Dead ratio is 2:1, U16 pin 13 is active and FF U3A outputs through the divide-by-2 circuit U10 to send MOD DECADE OUT signal to the Meas and Dead Generation circuit (Sheet 2). This circuit also receives the various dead time control signals from U16 and from Dead Time Stop circuit of transistors Q1, Q2.

8-93. The Count Chain Clear circuit (Sheet 1) receives the $\overline{\text{K}}$ code from A3 HP-IB decoders to reset the circuit to determine when a measurement starts. This reset causes a programmed number, such as D2M1EØK to be entered immediately.

8-94. When external dead time or programmed dead time is less than true dead time (time when no measurement is being made) the $\overline{\text{S2}}$ status signal is sent via the A3 HP-IB to the bus. (Sheet 2.)

8-95. An active $\overline{\text{HOLD BOTH}}$ signal from U12B to transistor Q6 causes the $\overline{\text{MEAS}}$ and $\overline{\text{DEAD}}$ OUTPUT signals to rise to ground level.

8-96. The DELAY ACCUM signal from A5 System Control inhibits the $\overline{\text{S2}}$ status signal if data is not being transferred.

8-97. A7 Converter Board

8-98. The Converter board consists of two switching regulators, one that takes the +15V @ 1A from the mainframe and converts it to +5 @ 2.4A maximum rating. The other regulator takes the +20V @ 1/3A from the mainframe and converts it to 5V @ 1A. Essentially the two switching regulators are identical except for differences in some of the component values, as shown in *Figure 8-11*.

8-99. Since the two regulators have identical circuit operation, only the +5V A regulator will be described. To provide the +5V A output, transistor Q5 must be turned on by the control circuit, in such a manner that it is turned on and then turned off sharply, so that Q5 is operated either saturated or all the way off. When +15 volts is applied through transistor Q5, current flows through inductor L4 to charge capacitor C6, when there is a load on the output. The current flow will increase gradually until the control circuit (described later) turns off transistor Q5, at which time the current will decrease gradually due to the effect of the inductance of L4 and the current supplied by diode CR8. Capacitor C6 is a special design with two leads connected to each side. This type of connection forces the current through the capacitor and effectively filters RF. Diode CR9 is a clamping diode (6V zener) to provide protection to the circuit if transistor Q5 does not turn off. If the current through inductor L4 increases beyond a set limit, the 5345A mainframe current limiting circuit will go into effect.

8-100. The test points at the top of the board are provided as a convenience when checking voltages. For detailed tests (such as noise tests) the board should be placed on an extender board so the probing can be at the connector.

8-101. CONTROL CIRCUIT. Transistor Q6 is a booster that supplies the current for the base of Q5. The base of transistor Q6 is driven by Q7. The output voltage +5V A is compared by a line that comes from the junction of the collector of Q5 and L4 to indicate when the output voltage has dropped below a reference voltage or when its above. When its below, Q5 is turned on and when its above, Q5 is turned off. The 5-volt reference voltage is from the 5345A mainframe. The voltage comparison is made by operational amplifier U3 which controls transistors Q7 and Q6 to turn Q5 on and off. When the +5V A output voltage increases to approximately +5.07V, the control circuit acts to turn off transistor Q5 and when the output voltage decreases

to approximately 4.93V, the control circuit acts to turn on transistor Q5 again. Diode CR10 clamps the output of U3 to go not lower than -0.7 volt, so the output of U3 will go from -0.7 to +12 volts. Diodes CR12 and CR13 are used as clamping diodes to provide a +12V and a -12V operating voltage to U3. Resistor R20 in the emitter circuit to transistor Q7 is a current limiting resistor to limit power dissipation in Q7. Capacitor C7 is used to minimize ringing in the circuit. Resistors R17 and R18 provide leakage current for transistors Q3 and Q6 so that the leakage current is not drawn from the emitter-base junction which would turn on the transistors at the wrong time. Resistor R19 is provided as a current sink to turn on the base of Q5.

8-102. Inductor L3 and capacitor C5 act to keep large voltage spikes from getting back to the 5345A mainframe via the +15V supply.

8-103. Capacitor C8 and resistor R30 provide an RC time constant circuit to prevent initial surges of current drain from the 5345A mainframe +15V supply when power is first applied to prevent exceeding the current capacity of the mainframe.

8-104. POWER FAIL INDICATOR CIRCUIT. The +5V A output voltage is monitored by pin 2 of operational amplifier U4. When the +5V A output drops to approximately 4.5V the polarity between pins 2 and 3 of U4 will result in an output from U4 that will turn on transistor Q8 and turn on indicator DS2.

8-105. +5B OUTPUT CIRCUIT. The +5B circuit differs only in some of the component values. Resistor R8's value differs primarily to minimize the current in transistor Q3. Resistor R16, capacitor C2 differ in the control circuit. Operational amplifiers U1 and U3 are connected to different operating voltages. U3 uses + and -15 volts so if +15V goes down, so does U3. In the case of U1, it is connected to -15V and a +20V, so if the +20V goes down so will U1. So both U1 and U3 will not go down if +15V does. The value of R1 differs from that of R28 for the op amps. If the +15V is down, the +5VB will not be. Then either one or the other LED fail indicators will be on at a time to indicate if the +5VA or +5VB circuit is down (helps in troubleshooting).

8-106. The purpose of CR14 is to bleed off capacitor C8 at a higher rate in case of power fail, so when the power comes back on, transistor Q5 is not turned on for too long a period of time which would result in folding back the mainframe current due to excessive current drain. (5VA) 5VB has similar circuit.

8-107. A8 Memory

8-108. The A8 Memory board contains 16 RAM's, U1 through U16, as shown in *Figure 8-12*. RAM's U1, 3, 5, 7, 9, 12, 14, and 16 are referred to as the upper K and RAM's U2, 4, 6, 8, 10, 13, 15, and 17 are referred to as the lower K. Each group of RAM's contains 1K 8-bit bytes of memory. Each RAM contains 1024 cells and stores one-bit in each cell. The address lines, control lines, and data inputs come from the A4 Memory Control. Address lines A1 through A10 are connected in parallel to each RAM's AØ through A9 line, respectively. Each of the data input lines, DI1 through DI8 is connected to one of the upper K and one of the low K RAM's. Each of the data out lines DO1 through DO8 is connected to one of the upper K and one of the lower K RAM's. The selection of the upper K or lower K group of RAM's is controlled by the A11 line and the Module Select 1 line (MS1) through gates U11A,B, and C, For the first 1024 addresses, line A11 will be a logic Ø and after the first 1024 address, A11 will be a logic 1, so either the lower K or the upper K group of RAM's will be selected respectively. As the address is incremented the data is entered through the DI1—DI8 lines. The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) line. With $\overline{WE}$ held LOW and the group selected, the data is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the group selected. Data is read out into the DO1—DO8 lines to the A3 HP-IB board.

8-109. The F1 line supplies a ground connection to the A4 Memory Control to indicate that the Memory board is installed. The F2, F3, and F4 lines serve the same purpose (if additional

memory board options are installed) for memory boards A9, A10, and A11 installed in the XA9, XA10, and XA11 slots, respectively. The additional memory boards must always be installed in the next higher numbered slot before they will operate (slots must be used in numerical sequence when additional memory boards are installed). In addition, the Module Select line is labeled MS2, MS3, and MS4 for boards installed in slots XA9, XA10, and XA11, respectively.

Example Conversion Chart

DECIMAL	HEXADECIMAL	OCTAL	BINARY
00	00	000	00000000
01	01	001	00000001
02	02	002	00000010
03	03	003	00000011
04	04	004	00000100
05	05	005	00000101
06	06	006	00000110
07	07	007	00000111
08	08	010	00001000
09	09	011	00001001
10	0A	012	00001010
11	0B	013	00001011
12	0C	014	00001100
13	0D	015	00001101
14	0E	016	00001110
15	0F	017	00001111
16	10	020	00010000
17	11	021	00010001
18	12	022	00010010
19	13	023	00010011
20	14	024	00010100
21	15	025	00010101
22	16	026	00010110
23	17	027	00010111
24	18	030	00011000
25	19	031	00011001
26	1A	032	00011010
27	1B	033	00011011
28	1C	034	00011100
29	1D	035	00011101
30	1E	036	00011110
31	1F	037	00011111

8-110. A12 Display Board

8-111. A12 Display board contains LED's and associated circuits for indicating the operating state of the 5358A at the front panel. The LISTEN, TALK, and OUTPUTTING DATA LED's are illuminated by signals from the A3 HP-IB to indicate when the 5358A has been addressed to talk or listen and when (if addressed to talk) data is being outputted.

8-112. The ACCUMULATING DATA LED is illuminated when a measurement has been initiated and N measurements are not complete. The signal to the LED is from A5 System Control and indicates when the 5358A has control over the 5345A.

8-113. The MEMORY FULL LED is illuminated by a signal from A4 Memory Control to indicate that Memory is full.

8-114. A13 BNC I/O Board

8-115. The A13 board mounts the BNC connectors ACCUM TRIG IN connected to A5 System Control, and the SAMPLE TIME (MEAS/DEAD) and DEAD TIME (STOP, START) connected to A6 Gate Control.

8-116. DIAGNOSTICS AND TROUBLESHOOTING

8-117. Troubleshooting

8-118. The diagnostic test (refer to paragraph 4-8 through 4-11 for instructions on running the Diagnostic Test) for the 5358A is divided into 17 different test sections; each test section is dependent on the successful completion of one or more of the previous test sections for part of its successful completion. For example, Test Section 2 tests for Memory-Clear operations, but relies on the successful completion of Test Section 1's test of the HP-IB listen and talk circuits. Refer to *Figure 4-1* for equipment set-up and address switch settings.

8-119. *Table 8-3* is a list of the diagnostic test sections and the principle test performed by each test section, on the 5358A:

Table 8-3. Diagnostic Test Sections

TEST SECTION	DESCRIPTION
1	HP-IB Basic Functions
2	Memory-Clear
3	Data Bits
4	Low Memory Address
5	High Memory Address
6	Memory Status
7	Memory Data
8	Formatter — LIFO
9	Formatter — ASCII
10	Gate Generator — Mantissa
11	Gate Generator — Exponent
12	ACCUM — HALT
13	Mainframe Data Transfer-Bits
14	Mainframe Data Transfer — T Digits
15	N Counter Digits
16	Service Request and Status Byte
17	Dead Time

8–120. As each of the Test Sections is being run, the section number is listed on the printer to provide a record of the test conducted. *Table 8–4* is a sample listing obtained using a 9871A Printer, indicative of the successful completion of the Diagnostic program:

Table 8–4. Successful Diagnostic Printout

```
5358A DIAGNOSTIC 05358-16001 rev A
MEM SIZE  4096
TESTING IN SECTION  1
TESTING IN SECTION  2
TESTING IN SECTION  3
TESTING IN SECTION  4
TESTING IN SECTION  5
TESTING IN SECTION  6
TESTING IN SECTION  7
TESTING IN SECTION  8
TESTING IN SECTION  9
TESTING IN SECTION 10
TESTING IN SECTION 11
TESTING IN SECTION 12
TESTING IN SECTION 13
TESTING IN SECTION 14
TESTING IN SECTION 15
TESTING IN SECTION 16
TESTING IN SECTION 17
TEST COMPLETE
```

Errors, if any, are listed under the section number, giving the test (and subtest) number at which the error occurred.

8–121. The following pages explain each of the 17 Diagnostic Test Sections in order from 1 to 17. An explanation of error messages can be found in the troubleshooting procedure which follows each test section explanation. Refer to *Table 1–3* for a list of recommended test equipment.

8–122. Basically, there are two types of error messages. The first type is a failure message which means that data received from the 5358A is not exactly the same as the data the 9825A expected to receive. The following is a sample listing of several data failure messages:

```
TESTING IN SECTION  1
FAILED TEST #  1.2    ER=          4    AR=          0
FAILED TEST #  1.4    ER=          4    AR=          0
FAILED TEST #  1.8    ER=          1    AR=          0
```

The general format of this type of error message follows:

"FAILED TEST # n.m.p."	indicates the error occurred in test section n at test m and at subtest p where n, m, and p are integers.
"ER = 9"	indicates what the Expected Result for the test is. "9" may be a Status Byte in octal or data (9 is an integer) in octal or decimal.
"AR = r"	indicates what the Actual Result is. To pass the test (and subtests) AR = ER (r is an integer).

8–123. The second type is an Input/Output error. There is a statement (time statement) in the diagnostic program which tells the 9825A to wait so long for an input from the 5358A when the 9825A is the listener and the 5358A is the talker. If the 9825A does not receive any data from the 5358A within 1 second, the 9825A will print an I/O error. This statement is needed so the program will continue running; otherwise, the program would stop and require operator assistance. The following is a sample listing of some I/O errors:

```
TESTING IN SECTION  2
I/O ERR TEST#  2.1   ER=          10    AR=          0
I/O ERR TEST#  2.2   ER=           0    AR=          0
I/O ERR TEST#  2.3   ER=           0    AR=          0
I/O ERR TEST#  2.4   ER=           0    AR=          0
```

The items printed on each line have the same meaning as for the data failure messages. Note that an I/O error may occur even if AR = ER.

8–124. Since the 5358A is a software-controlled instrument, effective troubleshooting requires a thorough knowledge of both hardware operation and program execution.

8–125. 9825A Calculator Display Descriptions

8–126. Paragraphs 8–127 through 8–131 describe the meaning of displayed information (prompts) that occur during the test.

8–127. ENTER PRINT DEV ID # <current value>. This display is the print device ID #, composed of two parts: the calculator I/O select code and the HP-IB address. The select code is a decimal integer number from 2 through 15 (which is determined by the position of the select code switch located on the top side of the interface card connecting the calculator to the printer). The HP-IB address is a decimal integer from 00 through 15 and is determined by the printer Option 001 Interface assembly (refer to printer option manual for details). A default value (normally preset) is preprogrammed and is displayed as part of the prompt. If this value is acceptable, press CONTINUE key without keying in a number. When the normally preset value is not used:

a. If the printer is a 9866A, enter its I/O select code number (normally 6), then press CONTINUE key.

b. If the printer is a 9871A, enter the select code with the printer HP-IB address number (normally 701), then press CONTINUE key.

8–128. ENTER 5358A DEV ID # <current value>. This displays the 5358A device ID #, which is determined by the selection of the HP-IB address switches A1 through A5 at the rear panel. A default value (712) is preprogrammed and is displayed as part of the prompt. If this value is acceptable, press CONTINUE without keying in a number. If the normally preset value is not used, determine the HP-IB address by referring to Section III of this manual. Select the Listen Data address. Next, enter the I/O interface select code, joined with the two-digit decimal HP-IB address number, as follows:

Enter:
ccdd CONTINUE for 5358A (Default value is 712).

8–129. ENTER 5345A DEV ID # <current value> display. To default this entry, press CONTINUE as in preceding paragraph. If default is not used, determine the HP-IB address by referring to the address table found in Section III of this manual or to the 5345A manual, Remote Programming section. Select the Listen address corresponding to a noncomputer dump Talk mode. Next, enter the I/O interface select code to be joined with the two-digit decimal HP-IB address number as in the previous paragraph (Default Value is 710).

8–130. 5358A DIAGNOSTIC rev <current revision>. The revision number is displayed to identify the data of the diagnostic software. (This information can be helpful when in communication with HP service offices regarding possible problems.) Press CONTINUE key. This allows the diagnostic program to start. The printer should print:

5358A DIAGNOSTIC rev <current revision>
MEM SIZE 2048 (or 4096, 6144, 8192)
TESTING IN SECTION 1

This indicates the diagnostic program has started. If there are no failures, the program will continue to run without operator assistance, listing each section by number at the beginning of each new section (e.g., TESTING IN SECTION 9). At the end of the diagnostic program,

TEST COMPLETE

will be displayed and printed.

8–132. Special Function Keys

NOTE

Refer to *Figure 4–2* for a picture of the Special Function Keys Overlay for the Diagnostic program.

8–133. SUPPRESS PRINTING OF ERROR MESSAGES. Error messages will continue to print until the condition causing the error is corrected or testing that may be causing the particular error is completed. To discontinue printing of errors, press special function key f_7 for SUPPRESS PRINT. This will suppress all errors so that errors in subsequent sections will not be recorded. To activate error printing, press SHIFT key and special function key f_7, simultaneously.

8–134. HALT PROGRAM. To halt the test in progress in an orderly manner, press SHIFT key and special function key f_5, simultaneously. The program will usually stop immediately. If the printer is in the process of printing a line, it will be allowed to complete the line. In the case of the 9871A Printer, the printer has a data buffer which will be emptied. The STOP key will also stop the program in much the same way as the special function HALT key; however, in some cases, the halting of the program is not in an orderly fashion and could cause invalid errors. In a few cases, the HALT or STOP keys will not respond to the touch of the key and the RESET key must be pressed. The nonresponse is usually due to an I/O problem and can only be released by the RESET.

8–135. LOOP ON ALL TEST. Program may be activated to continue to run through all of the tests repeatedly until halted (i.e., after section 16, next section is 1, 2, 3, etc.). Press special function key f_{10} for LOOP ALL TEST. This mode may be deactivated by pressing SHIFT key and special function key f_{10}, simultaneously. The program will terminate after next test section 17 with a TEST COMPLETE message.

8–136. STOP ON FAILURE. Program may be activated to stop after each failure. Press special function key f_8 for STOP ON FAILURE. This function is useful during "LOOP ALL-TEST" or when operator's attention is not available to prevent excessive paper from being consumed due to an error. Program may be continued until next error by pressing CONTINUE key. This mode may be deactivated by press SHIFT key and special function key f_8, simultaneously, anytime. Starting the program from the RUN key will automatically deactivate this mode.

8–137. f_{11} EJECT PAGE. (Applies to 9871A printers only.) To eject the paper to a new page, press special function key f_{11} for EJECT PAGE. The tear point can be positioned at the top of the printer carriage, then RESET key pressed.

8-138. START, RESTART, OR CONTINUE PROGRAM, as follows:

a. Start program action is required only if the RESET key has been activated. Press RUN key. The program will start with the display — ENTER PRINT DEV ID # <current value>.

b. Restart Program action is required when program has completed the test, a HALT or a STOP has been activated. Press special function key f_5 for RUN ALL TEST. Note that an error will occur if the program has not been started from the beginning previously.

c. Continue Program action is required only when the STOP key or special function key f_8 STOP ON FAILURE has been activated. Press CONTINUE key. Note that, if the STOP ON FAILURE mode is still active, the calculator will stop running the program on the next failure.

8-139. f_0 DISPLAY TEST #. Program may be activated to indicate the specific test number. Press special function key f_0 for DISP TEST #. the display will show, for example:

SEC # 5 TEST # 298 SUB # Ø

Each time the special key is pressed, display is updated to show the most recent test number. This information is convenient in running the memory test, sections 4, 5, and 7, when memory size is large, for it gives the operator an indication that the test is proceeding smoothly.

8-140. f_6 PRINT ALL. Program may be activated to print the results of each test. Press special function key f_6 for PRINT ALL. Printer will respond by printing, for example:

4.51 ADDR = 62 ER 62 AR 62

This information is convenient to use in much the same way that the DISPLAY TEST # is used, to indicate to the operator that the test is proceeding smoothly. This mode will continue until deactivated by pressing SHIFT key and special function key f_6, simultaneously. Starting program from RUN will also deactivate this mode.

8-141. f_4 RUN/LOOP SPECIFIED SECTION. Program may be activated to run one or more sequential test sections. If one test section is specified, the program will automatically loop within that test section, printing the test section number only once. When more than one test section is specified, a TEST COMPLETE message will be given at the completion of the last test section specified, unless the LOOP ALL TEST is activated. Press special function key f_4 for RUN/LOOP PART. The display will respond:

ENTER <SEC #> .<TEST #> | <SEC #>

<SEC #> means the one or first test section number to be run. Test sections must be specified in sequential order (i.e., if section 2 to 4, then 2 must be entered). .<TEST #> is optional and allows the operator to specifiy a particular test # within a section. It is useful primarily for maintenance; for example: 2.4 where .4 is the test number. <SEC #> is optional and is used to specify the second test section number. Wraparound section numbering is not allowed (i.e., 15 through 20). Note that the comma is used to separate the two section numbers. After entering test section number(s), press CONTINUE key. To terminate this mode in cases where only one test section is specified, press SHIFT key and special function key f_4, simultaneously. The program will terminate with a TEST COMPLETE message at next completion of the section. This mode is automatically terminated by a HALT and RUN/LOOP PART or RUN ALL TEST or by a RESET/RUN operation.

8-142. f_9 LOOP ON FAILURE. The program may be activated to loop on the the test which fails next. This is primarily useful for troubleshooting, but is not effective for each test section because of the structure of the test.

8-143. SHIFT f_{11} CLEAR ALL. Press SHIFT key and f_{11}, simultaneously, as a master clear for all of the function keys whose shifted mode contains a clear function (i.e., keys f_4, f_6, f_7, f_8, and f_9).

8–144. SHIFT f_0 END PROGRAM. Special function key provided for loading the directive program from the tape cassette and starting the program. This is a return to the program which was described in the loading procedure in paragraph 4–12. The calculator must be in a HALT condition prior to actuating the END PROGRAM function. To END PROGRAM, press SHIFT and f_0 keys , simultaneously.

NOTE

For a listing of the diagnostic program, refer to paragraph 4–22.

8–145. Test Section 1 (HP-IB Basic Function)

8–146. This section tests the A1 HP-IB input board and A3 HP-IB control board for the ability to be addressed to listen, unlisten, serial poll, talk, and untalk. Completing these functions indicates that the 5358A is able to pass data to and from the 9825A calculator.

8–147. There are nine tests in this section as listed in *Table 8–5*. For tests one through six the 9825A interface card status byte is read for status of the NDAC, NRFD, and DAV lines after transmission of the address message. A result of octal 0 (all three handshake lines are inactive) indicates the HP-IB is in an idle state as should be after transmission of an UNLISTEN or a SERIAL POLL ENABLE command. A result of octal 4 (binary 100) indicates the NDAC line is active with NRFD and DAV inactive, therefore the 5358A is ready for data. Generally, the 5358A should be ready to receive data after it has been addressed to listen at either one of its listen addresses (data address or program address).

Table 8–5. Test Section 1 Tests

TEST	ADDRESS MESSAGE SENT TO 5358A	NDAC	NRFD	DAY	I/O FLAG	PRINTOUT CODE
1.1	Unlisten	0	0	0		0
1.2	Lower listen address	1	0	0		4
1.3	Unlisten	0	0	0		0
1.4	Upper listen address	1	0	0		4
1.5	Unlisten	0	0	0		0
1.6	Serial poll enable	0	0	0		0
1.7	Untalk				0	0
1.8	Upper talk address				1	1
1.9	Untalk				0	0

8–148. Tests seven through nine check the ability of the 5358A to be a talker in the serial poll mode. The address message of either talk or untalk is sent to the 5358A, the 9825A interface card is instructed to read data from the 5358A. When the 5358A is addressed to untalk, data should not be received by the interface card and the interface I/O flag should indicate a BUSY condition. When the 5358A is addressed to talk, the I/O flag should indicate a READY condition. The talk test (1.8) requires the 5358A to be in the serial poll mode as programmed in test 1.6.

8–149. Troubleshooting Test Section 1

8–150. Because test section one is checking the 5358A's HP-IB basic functions, only those instruments shown in *Figure 4–1* should be connected to the HP-IB bus.

8–151. The serial poll enable test is used to check the status byte of the 5358A. The upper listen address (data address) is used to send data to the 5358A. The lower listen address (program address) is used to send program codes to the 5358A.

8-152. The states of the three handshake lines NDAC, NRFD, and DAV are used to check the mode of the 5358A. For tests 1 through 6, the expected result and actual result will be expressed in octal form and will show the condition at the three handshake lines (as shown in *Table 8-5*). For tests 7, 8, and 9, the I/O flag in the 9825A HP-IB interface card is examined for the condition of the 5358A.

8-153. The RUN/LOOP part key f_4 is effective in this section. Looping on a particular test is helpful in creating a static condition for troubleshooting. Loop in test 1.6 is not effective because the test is dependent on a previous set condition. Loop on any of the other 8 tests, however, is effective.

8-154. A MEMORY FULL or ACCUMULATING DATA condition of the 5358A could also cause an error by indicating a NRFD (not ready for data) condition.

8-155. For errors in tests 1, 2, 3, 4, and 5, look at the handshake circuitry and listen flip-flop A2U12 and A2U16B. For errors in tests 6, 7, 8, and 9, examine the talk flip-flop A3U16A.

8-156. Test Section 2 (Memory Clear)

8-157. This section tests the ability of the 5358A to receive data and to send the status bits which indicates the empty and the not empty memory conditions. This test section checks the functions of the A3 HP-IB control assembly and A4 Memory control assembly to receive, store, and clear one-byte of data and to set, clear, and send the memory status bits of the 5358A status byte.

8-158. The 9825A sends a HALT (H), an output format code, and a RESET (R) (clear memory) command to the 5358A. The HALT disengages any previous data transfer from the 5345A while the format command programs the HP-IB assembly to minimize any additional circuits to be tested in Test Section 3. The initial RESET command clears memory, in case memory was left full from a previous test section because a memory full condition would not allow the 5358A to receive additional data.

8-159. Test Section 2 consists of four tests as listed in *Table 8-6*. One data byte, arbitrarily chosen as octal Ø, is sent to the 5358A. During test one, the memory status should be <1/2 full (not empty). On tests 2, 3, and 4, a program code message is sent, following the data byte, to clear memory in one of three ways: Select Device Clear (SDC), Reset (R), and Device Clear (DCL). Testing the status byte following the clearing of memory should indicate an empty condition.

Table 8-6. Test Section 2 Tests

```
SEC  2

          2.1   ER=      10   AR=      10
          2.2   ER=       Ø   AR=       Ø
          2.3   ER=       Ø   AR=       Ø
          2.4   ER=       Ø   AR=       Ø
```

8-160. Troubleshooting Test Section 2

8-161. The 5358A can be reset in 3 ways. These are RESET (R) (memory clear), Select Device Clear (SDC), and Device Clear (DCL). These signals are generated on the A3 (HP-IB) board primarily by A3U25 and A3U29.

8-162. RUN/LOOP PART f_4 is effective on three (2.2, 2.3, and 2.4) tests. Test 2.1 has no reset statement so eventually memory goes full stopping the 9825A.

8-163. Loop on Test 2.2 will activate the memory clear circuitry on the A3 and A4 boards. The memory clear (R) signal originates from the program decoder A3U24 Pin 13.

8-164. Loop on Test 2.3 will activate the memory clear circuitry via the Selective Device Clear signal from A3U25.

8-165. Loop on Test 2.4 will activate the memory clear circuitry via the Device Clear signal from A3U25.

8-166. The Error Printout message gives the expected result and the actual result of the STATUS BYTE in octal form. If the expected and actual result are converted to binary form, the difference between STB4 and STB5 can be seen. With this information, the troubleshooting procedure is to follow STB4 and/or STB5 from the output A3U28 back to the origin at A4U36.

8-167. The areas of possible malfunction are the A3 board STATUS BYTE circuit, the decoding of R, SDC, or DCL on the A3 board, the EMPTY/FULL circuitry on the A4 board, or the write (wrt) into memory and clear memory cycle.

8-168. Test Section 3 (Data Bits)

8-169. This section tests the ability of the 5358A to receive, store, and send a data byte. Data is generated by setting one of the eight-data bits to a logic 1 and the remaining bits to logic Ø to test one line of the eight-data lines at a time. Completion of this section verifies all eight bits of the data byte for shorts or opens. The data path is through the A3 HP-IB, A4 Memory Control, A8 Memory (address location Ø only), and A3 HP-IB format and output section.

8-170. The 5358A is initialized by sending the nonreverse, non-ASCII (first in first out binary data) format code F2. The digit transfer code of T1 is also sent to minimize the additional circuits to be tested in later sections.

8-171. This test section consists of nine tests listed in *Table 8-7*. For every test, an expected result (ER) is assigned and a memory reset is sent to the 5358A. The expected value generated is such that a logic 1 is in the bit position corresponding to the test number, counting from the least-significant-bit, with the remaining seven bits assigned a logic Ø. This allows each data line to be individually tested for both a logic 1 and Ø state. Test 9 generates all logic Ø's. The expected value is sent to the 5358A, stored in the first address of 5358A memory and read back into the 9825A as the actual result.

Table 8-7. Test Section 3 Tests

```
SEC  3

          3.1   ER=      1   AR=      1
          3.2   ER=      2   AR=      2
          3.3   ER=      4   AR=      4
          3.4   ER=     10   AR=     10
          3.5   ER=     20   AR=     20
          3.6   ER=     40   AR=     40
          3.7   ER=    100   AR=    100
          3.8   ER=    200   AR=    200
          3.9   ER=      0   AR=      0
```

8-172. Troubleshooting Test Section 3

8-173. The data lines are being checked from the A3 board through the A4 board to the A8 board and from the A8 board back through the A3 board buffer (A3U48, U46).

8-174. Each test except test 9 tests one of the eight data bit lines by setting it high and the remaining seven low.

8-175. The error printout is in octal form. If changed to binary form, the logic 1 is in the bit position corresponding to the data bit being tested. Test 9 sets all data bit lines to logic Ø.

8-176. RUN/LOOP PART f_4 is effective and allows the bit signal to be followed through the 5358A. Possible areas of malfunction are the read/write or clear cycle on the A4 board, or the load/unload circuitry on the A3 board. The read and the write address on the A4 board (U23, U29, and U20, U26 respectively) should toggle between address 0000 and 0001. Any other address indicates a malfunction in the read/write cycle.

8-177. Test Section 4 (Low Memory Address)

8-178. This section tests the ability of the 5358A to receive, store, and send a block of data. A block of data is defined as 256 bytes. Each byte of data is unique in order to detect errors caused by mixing data within the block of data. The first half of Section 4 consists of writing and reading one byte of data at a time for a total of 256 times. This allows the address read and write counters to address all the first 256 memory cells. The second half of Test Section 4 consists of writing a full block of 256 bytes of data at one time and then reading back one byte at a time. In this way separate operation of the write and read address counters and memory cells can be verified. Completion of this test verifies the eight-least-significant (low order) memory address lines addressing main memory for both read and write operations and the first 256 bytes of memory.

8-179. The 5358A is initialized by sending the nonreversed binary format code F2 and a reset memory command (R) (sets memory address write and read counters to zero). Data is generated as a binary number between Ø and 255 and stored in the string array D$. The data corresponds to memory addresses Ø through 255 for convenience of error detection.

8-180. Test Section 4 is defined as being in two groups. The first group, consisting of Tests 1 through 256, sends one binary number corresponding to the test number minus 1 (that is address Ø through 255) to the 5358A and reads one binary number back from the 5358A. The error comparison is made after each write and read. The second group of tests starts at test number 257 by first sending a Select Device Clear (SDC) to the 5358A which should reset memory (set both read and write address counters back to zero). Data from the string array D$ is sent to the 5358A as a block, that is 256 bytes of data are written into the 5358A memory. Then one byte of data is read from memory and compared with the expected result for an error. Test numbers 258 through 512 continue this process of reading one byte of data and comparing the actual result to the expected result.

8-181. Troubleshooting Test Section 4

8-182. The lower eight address lines (A1 through A8) are being checked for short and opens from where they originate on the A4 Memory Control board through the (A1) Motherboard to the A8 (A9, A10, A11) Memory board(s).

8-183. This test is grouped into two types of tests. In the first group (Test 1 to 256), the 9825A writes a byte to the 5358A and immediately reads it back. In the second group (tests 257 to 512) the 9825A first writes a block, which is defined as 256 bytes (test 257), into the 5358A. Then the 9825A reads (258 to 512) from the 5358A one byte at a time.

8–184. RUN/LOOP PART f_4 is effective for Tests 1 to 256. The error printout shows the test number in decimal and the address, expected result (ER) and actual result (AR) in octal. By changing the ER and AR to binary form, the faulty address line(s) can be isolated.

8–185. RUN/LOOP PART f_4 on Tests 257 to 512 is not effective. During test 257, after a memory clear, one bock (256 bytes) of data is written into memory. At this time, the write address counter has counted to 256, while the read address counter is at zero. Tests 258 to 512 will be reading from the 5358A one byte at a time and at the same time the read address counter will be incremented once for each read (tests 258 to 512).

8–186. The areas of possible malfunction in tests up through 256 are in the data cells of the A8 Memory board. For failure of tests 257 to 512 the problem may be the address multiplexer or the address lines on the A4 Memory Control board.

8–187. Test Section 5 (High Memory Address)

8–188. This section tests the higher order address lines (A9 to A11, MS1 to MS4) and corresponding memory cells. This section is similar to Test Section 4. Known data is written into the 5358A memory at one time and then read back from memory and checked against the expected value. It is assumed but not previously tested, the high address memory cells are functioning correctly.

8–189. The 5358A is initialized for a digit transfer of 1 and the programming format code F2 specifying the binary nonreverse format. An "R" (memory clear) command is sent to start memory at a known point. All the data is written into memory at one time. The data is then read one-byte at a time and compared with the expected value.

8–190. Troubleshooting Test Section 5

8–191. RUN/LOOP PART f_4 is not effective because all addressing must start with a reset. Stop on failure f_8 is effective, but the address on the A4 memory control board points to the address indicated by the error printout plus one.

8–192. After stopping the program on an error, determine by examining MS1 to MS4 on the A4 Memory Control board U31, which memory board (A8, A9, A10, or A11) is being addressed. If there is only 2K of memory (one memory board installed) the defect possibly exists in the address lines A9 through A11 or the data cells in the upper K (top row of 8 IC's) on the A8 Memory board. If there is more than one memory board installed, there may be a problem in the MS1 to MS4 circuitry. The empty-full circuit on the A4 Memory Control can also cause an error if memory becomes full prematurely.

8–193. Test Section 6 (Memory Status)

8–194. This section tests the memory status and the EOI (HP-IB line that indicates EOF, end of file). Memory status is generated on the Memory Control board empty/full circuit, and modified on the HP-IB board to include HP-IB data output buffer empty. EOI is the result of sending the last byte of data in the binary format only. The empty/full circuit has been partically checked in the low and high address test (Test Sections 4 and 5) to the extend that memory did not go empty prematurely. The 5358A is initialized with a memory clear "R" and binary nonreversed format (F2). Memory address is calculated for 1/2 full and full, for a given memory size M. The memory size is specified by the operator during the start-up of the diagnostic.

8–195. Memory status is first read to confirm that memory is empty as the result of the memory clear during the initialization. Next, one byte is sent to the 5358A and Status is checked again. Status should now read ≤1/2 full. Again one byte is sent to the 5358A and Status is read. This

continues until memory is full, checking Status after each write. At memory >1/2 full, Status changes and the program assigns a new expected value. When memory is full, Status is checked for a full value.

8-196. Finally, one byte is read from memory, and Status is checked for >1/2 full, This process continues through ≤1/2 full until memory is empty. During the entire read portion of the test, the EOI line is checked via the calculator EOF status for an indication of an "end of file". One the last byte read from the 5358A, the EOF status should indicate end of file.

8-197. Troubleshooting Test Section 6

8-198. The memory status is generated on the A4 Memory Control board and is output through the A3 HP-IB board. The affected status bits are STB4 and STB5. Depending on the state of these bits, memory is indicated to be full (Bit 5=1, bit 4=1), >1/2 full (1,0), ≤1/2 full (0,1) or empty (0,0). The error message contains the test number, the address, the expected result (ER) and the actual result (AR).

8-199. By using the STOP ON FAILURE (4_8) key, the program can be stopped on the error creating a static condition. After status has been determined as to which state it should indicate (by dividing the printout address by the total amount of memory) the malfunction can be traced from the final output A3U28(4, 14) back to the detector circuit A4U39(1, 4).

8-200. Expected result (ER) 400 occurs when memory is empty (memory is empty and HP-IB storage buffer A3U48, U46 memory is empty). Status bits STB4 and STB5 are low and EOI (end of file) is high.

8-201. Test Section 7 (Memory Data)

8-202. This section tests the memory data cells for all of the memory. The data lines were tested in the DATA BIT TEST (Section 3). Data cells were tested indirectly during the Low and High address test (Section 4 and 6), however, in this section four different bit patterns are written into and read from the 5358A and compared. These bit patterns are shown in *Table 8-8*. The 5358A is initialized for a format of binary nonreversed "F2" and memory is cleared.

8-203. The test section writes and reads one block of a known bit pattern at a time and compares known (expected result) with actual results. If a mismatch occurs, the test is incremented one at a time (the block is broken down byte-by-byte), looking for the error in data between known and actual, otherwise, the test is advanced by one block of data. After memory is compared for one-bit pattern, the bit pattern is changed and memory is checked again.

8-204. Troubleshooting Test Section 7

8-205. This section tests all the memory data cells. In order to do this, four-bit patterns are generated and written to the 5358A and immediately read back by the 9825A. The actual result (AR) is compared to the expected result (ER). If they match, the test is incremented. If a mismatch occurs, an error condition exists and an error message is printed.

Table 8-8. Section 7 Bit Pattern Tests

	B8	B7	B6	B5	B4	B3	B2	B1	Octal
Bit Pattern 1	1	0	1	0	1	0	1	0	252
Bit Pattern 2	0	1	0	1	0	1	0	1	125
Bit Pattern 3	1	1	1	1	1	1	1	1	377
Bit Pattern 4	0	0	0	0	0	0	0	0	0

8–206. The four bit patterns (bytes) generated and sent to the 5358A are listed in *Table 8–8*. These bit patterns are written to and read from the 5358A in a 256-byte block for all of memory. When each pattern has been successfully completed, the next pattern is generated and the test sequence is repeated. If an error exists, the test is incremented one address at a time, looking for the error in data between the expected result (ER) and the actual result (AR).

8–207. By using the STOP ON FAILURE key f_8, the process will stop one address after the error occurs creating a static condition making logic path tracing possible.

8–208. If all previous tests pass, then the data path through the A3 HP-IB board can be assumed to be operating correctly. The problem may be in the A4 address counter circuitry (if more than 2K memory is installed) or the A8, A9, A10, or A11 memory board or boards.

8–209. If the test stops on an error, the error printout shows at which address it is stopped (one address higher than where the error occurred), and the expected result (ER) and the actual result (AR) the 9825A received.

8–210. Starting with the address latch (A4U22, U25), verify the printout address with the actual address. The problem could be that the read-address counter (A4U23, U29) is not incrementing properly so the correct address location is not being accessed. If the addressing is working properly, the fault may be in the (A8) memory board or boards. By comparing the actual and the expected results (both in binary form), the bit in which an error exists (bit Ø through bit 7) can be detected. This will show which 2 of the 16 IC's on the A8 memory board are malfunctioning. By looking at the address (in decimal form) where the failure occurred, and comparing it with the total number of address possibilities (memory size), it can be determined which row (upper or lower K) of 8 IC's (on the A8 memory board) is being addressed.

8–211. Test Section 8 (Formatter — LIFO)

8–212. This section partially checks the capability of the 5358A (HP-IB board) to send data out through the HP-IB bus in different formats. The 5358A can send data in three different formats: binary nonversed, binary reversed, and ASCII. All previous sections used binary non-reversed format. This section tests the binary reversed (last in first out) format.

8–213. There are 15 tests in this section. The T-counter (the number of digits transferred counter) is set to the test number, e.g., for test 7, the T-counter is set to 7. The new circuits checked in this section include A3U41 used to decode the format program codes (FØ to F2). Also checked are the T-register (A3U43) and the T-counter (A3U53). Previous to this section T had a value of 1. This implies that the operation of U58 has been checked and verified. The buffer address counter (A3U44) and the buffers (A3U46, U48) are also checked for all possible addresses.

8–214. Troubleshooting Test Section 8

8–215. This section tests the T digit counters (A3U53, U58, U43) and the HP-IB storage buffers and counter (A3U48, U46, U44). The 5358A is programmed for FØ format (LIFO: last in, first out).

8–216. In the error message, the (1 to 15) represents the T-counter value. "T" digits are sent into the buffer and then out through the ASCII bus LIFO. This sequence is done three times for every "T" value. Two examples are given in *Table 8–9*.

8–217. LOOP ON TEST (Special Function key f_4) is effective. By looping on a particular test, correct operation of the T-register (A3U43) and the T-counters (A3U53, U58) can be verified by checking that the "T" number (test number) is present at the T-counters (A3U53(15, 1, 10, 9)) and A3U58(15). Also verify the TC=O (TP-5) is toggling. This signal is needed to tell the END OF READ FF)A3U65) that "T" digits have been transferred.

Table 8-9. Section 8 Test Examples

	Test No.	"T" Register	EXPECTED VALUE (ER)											
Example 1	8.3	3	3	2	1	6	5	4	9	8	7			
Example 2	8.4	4	4	3	2	1	8	7	6	5	12	11	10	9

8-218. Test Section 9 (Formatter ASCII)

8-219. This section tests the ability of the 5358A to output data through the HP-IB bus in the ASCII format (code f_1). All previous sections have been in binary output format.

8-220. There are 13 tests in section 9. The test number corresponds to the T-counter preset value (test 9.4, T=4). In each test the 5358A will send data out to the HP-IB bus. The data will be "T" digts (Time scale digits), then a comma, "T" more digits (event scale digits) a carriage return and a linefeed.

8-221. This coding is accomplished by the circuitry on the upper half of page 4 of the A3 board schematic. ASCII format status latch U66 and associated gates tell the circuits on the upper right of page 4 when to generate a comma, carriage return, and a linefeed.

8-222. Troubleshooting Test Section 9

8-223. This section tests the ASCII formatter (A3U66) and associated circuits. The purpose of the ASCII format status latch (A3U66) is to keep track of when, in the data output sequence, a comma, carriage return, and line feed, needed in the ASCII format, should be generated.

8-224. A typical example of the section printout is shown in *Table 8-10* (generated by pressing key f_6 print all). ASCII format is LIFO (last in first out).

Table 8-10. Printout Explanation

Section	Test	Subtest	ER	AR	ASCII Data (ER and AR)
9	1	6	63	63	3
9	1	7	54	54	,
9	1	8	62	62	2
9	1	9	15	15	CR
9	1	10	12	12	LF
9	1	11	65	65	5

8-225. The sequence starts with the T-counter being set to "T", and A3U66 being cleared by a load through A3U69(12). The load is also responsible along with read accept signal for loading "T" digits into the A3 buffer (U46 and U48). When "T" digits are loaded into the buffer and the T-counter at zero, the signal will then set the T-counter back to the "T" value.

8-226. Outputting data starts when unload (from A3U65(5)) is present at A3U46 and U48 and the address down-clock is present at A3U44(4) from A3U61(8). Because of the T signal from A3U66(6) to U54(4), the address down-clock will occur once for every two data accept clocks. With the T-counter being decremented once every data accept, the T-counter will go to zero but the address counter (U44) will only be half-empty. At this point the state machine (U66) will supply a comma to the bus. When the comma is accepted, the data accept will preset the T-counter and continue the sequence once more.

3–227. When the T-counter reaches zero, the address counter U44 will also be zero. This causes state machine U66 to output a CR (carriage return) and a LF (linefeed) to the bus.

8–228. Test Section 10 (Gate Generator — Mantissa)

8–229. This section tests the A6 gate control board. Specifically, the Mantissa portion of the gate signal generator will be stimulated. The Mantissa registers are A6U20 and U23 and the Mantissa counters are A6U19, U22, and U26. Because the 5358A generates a gate window for the 5345A, the 5345A must function with an external gate. This is the first section of the diagnostic that relies on the proper functioning of the 5345A (other than power supplies for the 5358A).

8–230. There are 21 tests in this section. Test 1 through 12 test one only of each of the 12 (3-by 4-bit) preset input lines to A6U19, U22, and U26. Tests 13 through 21 test U19, U22, and U26 with the same decade number sent to each. A typical example of the printout obtainable by pressing special function key f_6 print all is shown in *Table 8–11*.

Table 8–11. Section 10 Printout (partial)

Test	ER	AR
10.8	80	80
10.9	100	100
10.10	200	200
10.11	400	400
10.12	800	800
10.13	111	111
10.14	222	222
10.15	333	333

8–231. Along with the M-counters, the M-registers A6U20 and U23 are checked for proper operation and, except for the Exponent register and counter and the Dead Time register and counter, the remainder of the A6 board must operate for the input and output of the clock signals.

8–232. Troubleshooting Test Section 10

8–233. The 5358A is programmed, depending on the test, for a measurement gate window of a particular time interval in μseconds. This window is sent to the 5345A external Gate Control Input. The 5345A is programmed for TIME INTERVAL and EXTERNAL GATE. The 5345A then measures the length of the signal applied to the Gate Control Input. The result is displayed by the 5345A and sent on the HP-IB to the 9825A. This reading is compared to the expected result. If there is a mismatch, then an error condition exists.

8–234. Loop On Test f_4 is used, depending on the test number, verify that the M counters (A6U19, U22, U26) are set to the correct number. If not, suspect the M registers (A6U20, U23). If the correct number is being sent to the counters, check the borrow out of A6U26(13) and the succeeding load from A6U18(5). If all are functioning correctly, check the decade out of A6U14(1) and follow the signal through A6U10(5) and A6U1(11). The signal is now called MEAS and is output through the 5358A rear panel BNC. If this signal is correct then a problem exists in the 5345A mainframe.

8–235. Test Section 11 (Gate Generator — Exponent)

8-236. This section tests the exponent counter A6U14 and exponent register A6U15 on the A6 Gate Control board.

8-237. There are 8 tests in this section. The test number minus 1 is used as the exponent of the measurement time. With the mantissa set to 1, the exponent is set to Ø, 1, 2,...7. This is equivalent to measurement times of 1, 10, 100,...10^7 μs. *Table 8-12* shows all 8 tests in this section.

Table 8-12. Section 11 Tests

TEST	ER	AR
11.1	1	1
11.2	10	10
11.3	100	100
11.4	1000	1000
11.5	10000	10000
11.6	100000	100000
11.7	1000000	1000000
11.8	10000000	10000000

8-238. When the exponent counter counts down M to the E power an output occurs at U14(1) called Mode Decade Out. This signal ripples through and becomes the MEAS output.

8-239. Troubleshooting Test Section 11

8-240. Test Section 10 checked all circuits being stimulated in this test section except for the Exponent Counter and the Exponent Register.

8-241. By looping on a particular test, Run/Loop part, (special function key f_4), the Exponent Register (A6U15) can be checked by verifying that the correct value of the exponent is present at the outputs (pins 2, 7, 10, 15). If the correct value is not present, and the clock is present (A6U15(9)), check U15.

8-242. If the correct value is present at the outputs of U15, check the Exponent Counter A6U14. First check pins 15 and 16 or U14 for levels of +5V and -14V respectively. Next, check the Reset Max (Pin 6) and the Ext. Input (Pin 3). If these inputs are in order, U14 is defective.

8-243. Test Section 12 (ACCUM-HALT)

8-244. This section tests mainly the A5 System Control board. More specifically it tests the ability of the 5358A to start an accumulation of data from the 5345A and to halt the accumulation.

8-245. This section consists of 9 tests. The tests with the expected and actual results and the commands sent to the 5358A are shown in *Table 8-13*. After the command in each test, the 9825A waits 175 milliseconds. The the 9825A reads the status of the 5358A memory. The memory status bits STB4 and STB5 are compared to expected results in the 9825A. If there is a mismatch then an error condition exists.

8-246. Note that this section is not concerned with the actual data transferred from the 5345A to the 5358A. The 5358A is being tested to see if it can be initiated, i.e., to start and halt an accumulation. This is checked by reading the memory status of the 5358A. If memory is empty then Reset (R), and clear (Device Clear and Selected Device Clear) are working. If memory is full then initiate (I) and trigger (Group Execute Trigger) are working.

Table 8-13. Section 12 Tests

SEC 12	Test	Expected Result	Actual Result	Command Sent to 5358A
	12.1	ER = Ø	AR = Ø	Reset Halt
	12.2	ER = 3Ø	AR = 3Ø	Reset Initiate
	12.3	ER = Ø	AR = Ø	Reset Halt
	12.4	ER = 3Ø	AR = 3Ø	Trigger
	12.5	ER = Ø	AR = Ø	Clear
	12.6	ER = 3Ø	AR = 3Ø	Trigger
	12.7	ER = Ø	AR = Ø	Device Clear
	12.8	ER = Ø	AR = Ø	Counted
	12.9	ER = 1Ø	AR = 1Ø	Reset Initiate Halt
NO ERRORS — TEST COMPLETE				

8-247. Troubleshooting Test Section 12

8-248. In this section, the different ways the 5358A can be initiated to start taking measurements are checked.

8-249. As can be seen in *Table 8-13*, an accumulate code is sent to the 5358A in tests 12.2, 4, and 6. LOOP ON TEST (Special Function Key f_4) is effective: follow the signal from where it is decoded on the A3 HP-IB board (U27(6)), to where it terminates on the A5 System Control Board (U6(10)) and becomes the $\overline{\text{ACCUM}}$ signal for the A4 Memory Control board.

8-250. Note that after each accumulation command when memory is full, a reset is sent to clear memory. This must be done so that a memory-full condition will not prevent the accumulation of data.

8-251. The last test (12.9) checks the HALT command "H". First an "R" is sent to clear memory followed by an "I" (initiate) which starts data accumulation followed by an "H" which halts data accumulation. When memory status is read it should indicate that memory is not empty but less than half-full (10).

8-252. Test Section 13 (MAINFRAME DATA TRANSFER BITS)

8-253. Test Section 13 checks the data bit lines from the 5345A mainframe to the 5358A Memory Control board (A4). These lines come into the Memory Control board on pins 4, 5, 6, and 9 of the A connector. They are labeled DRA, DRB, DRC, and DRD.

8-254. There are 12 tests in Section 13. They are divided into 3 groups of 4. The bit patterns (numbers) generated in each of the groups are the same: the difference is the power of 10 by which the numbers are multiplied. A listing of the tests are shown in *Table 8-14*.

8-255. Troubleshooting Test Section 13

8-256. Test Section 13 is checking the Memory Control board for the ability to accumulate known data from the 5345A mainframe. More specifically it is checking the operation of the data drive circuit on the A4 board. The data drive circuit consists of A4U17, 15, 16, 18, and 19. A4U16 and U19 have been previously checked as have half of A4U15 and U18 when data was sent to the 5358A via HP-IB to be stored in memory (Test Section 1). Now data is acquired from the 5345A so that the other half of A4U15 and U18 and U17 can be checked.

Table 8-14. Test Section 13 Printout

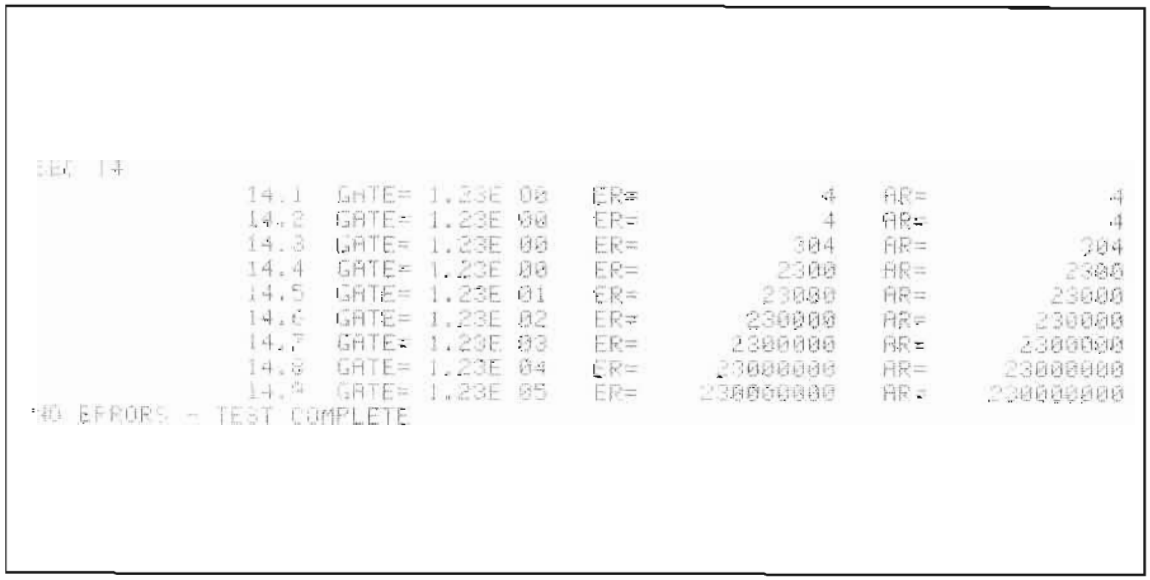
TEST	GATE	ER	AR	Date Line Tested
13.1	1.11E00	11100	11100	DRA
13.2	2.22E00	22200	22200	DRB
13.3	4.44E00	44400	44400	DRC
13.4	8.88E00	88800	88800	DRD
13.5	1.11E02	1110000	1110000	DRA
13.6	2.22E02	2220000	2220000	DRB
13.7	4.44E02	4440000	4440000	DRC
13.8	8.88E02	8880000	8880000	DRD
13.9	1.11E04	111000000	111000000	DRA
13.10	2.22E04	222000000	222000000	DRB
13.11	4.44E04	444000000	444000000	DRC
13.12	8.88E04	888000000	888000000	DRD

8-257. The tests (1 through 12) are set up so that only one of the four bits lines (DRA–DRD) are active at a time. LOOP ON TEST (f_4) is effective: for example, in test 13.3 line DRC should be active (toggling) and the remaining lines should be inactive. DATA CLK 1 (U17(9)) is needed to step the data through U17 for all tests.

8-258. Test Section 14 (MAINFRAME DATA TRANSFER-T DIGITS)

8-259. This section exercises and checks the Transfer counter (A5U8, U5) on the System Control board (A5). This Transfer counter is used to control the number of digits transferred from the 5345A to the 5358A. Section 14 contains 9 tests as shown in *Table 8-15*. The number of digits transferred (Transfer counter) is arbitrarily set equal to the test number. The first 4 tests have a programmed measurement time (gate window) of 1.23 x 10^0 μseconds. In the 5th through 9th test, the exponent of the measurement time is incremented one for each test. This is done so the more significant digits are accumulated as the programmed number of digits transferred increases.

Table 8-15. Section 14 Tests



8–260. Troubleshooting Test Section 14

8–261. The Transfer Counter is used to limit the number of digits to be transferred from the 5345A to the 5358A. This feature is available to save Dead Time (nonmeasurement time) and memory space. For example, if a measurement was made which gave 6 significant digits, 14 μs, and four bytes of memory can be saved by transferring only the 6 digits instead of all 13 available (7 leading Ø's).

8–262. By looping on a particular test (test number is the T-number) check that the T-number is present at the inputs of A5U5 and U8. If present, check the borrow's of each of the counters (pin 13), especially U5. U5's borrow signal goes through U7A and U7B and becomes the $\overline{\text{PI DUMP}}$ signal. This is the signal sent to the 5345A to start transferring data.

8–263. Test Section 15 (N-COUNTER DIGITS)

8–264. This section tests the N-counters A5U15, U18, U21, and U23 on the A5 System Control board. The N-counters control the number of measurements to be made. The N-registers A5U16, U19, and U22 are also being checked for proper operation. Status byte bit-6 (STB6, the N measurements complete signal) is also checked for proper operation. The 5345A is programmed for FREQ A, CHECK, GATE TIME MIN and must function properly.

8–265. There are a total of 26 tests in this section. The first 16 tests are used to check each of the 16 bits of the N-registers and counters. The remaining tests program the same decade number (1111,2222,....) into each of the 4 counters. This is done to make sure there is no interaction between any of the registers or counters. The complete printout of Section 15 is shown in *Table 8–16*. The first column is the test number, the second and third columns are the expected (ER) and actual results (AR), and the fourth column is the 5358A status byte in octal form. ER is the number sent to the N registers and counters. AR is the number of measurements that were actually made.

Table 8–16. Section 15 Test Printout

Test	Expected Result	Actual Result	Status Byte
15.1	ER = 1	AR = 1	152
15.2	ER = 2	AR = 2	150
15.3	ER = 4	AR = 4	150
15.4	ER = 8	AR = 8	150
15.5	ER = 10	AR = 10	150
15.6	ER = 20	AR = 20	150
15.7	ER = 40	AR = 40	150
15.8	ER = 80	AR = 80	150
15.9	ER = 100	AR = 100	150
15.10	ER = 200	AR = 200	150
15.11	ER = 400	AR = 400	150
15.12	ER = 800	AR = 800	150
15.13	ER = 1000	AR = 1000	150
15.14	ER = 2000	AR = 2000	160
15.15	ER = 4000	AR = 4000	164
15.16	ER = 8000	AR = 8000	164
15.17	ER = 1111	AR = 1111	160
15.18	ER = 2222	AR = 2222	164
15.19	ER = 3333	AR = 3333	164
15.20	ER = 4444	AR = 4444	164
15.21	ER = 5555	AR = 5555	164
15.22	ER = 6666	AR = 6666	164
15.23	ER = 7777	AR = 7777	164
15.24	ER = 8888	AR = 8888	164
15.25	ER = 9999	AR = 9999	164
15.26	ER = 1	AR = 1	150

This value depends on amount of available memory

8-266. The 5358A is programmed for a "T" of one (Transfer one digit). This is done so that one 9825A read corresponds to one measurement. The 5358A is also programmed for the "F2" format (binary nonreversed). The 9825A programs an N-number to the 5358A. Then the 5358A is sent an I command (initiate) to start counting and accumulate N measurements. The 9825A reads the data from the 5358A. The 9825A counts as it reads and when the 5358A's memory is empty, the 9825A compares the number of reads to the N-number. If they are not the same, then the N-counters are miscounting and an error condition exists.

8-267. Troubleshooting Test Section 15

8-268. By looping on a particular test and referring to *Table 8-17* for the ER (N-number), check to see if this number is at the inputs of A5U15, U18, U21, and U23 pins 15, 1, 10, and 9. If the correct number is not present at these inputs and the clocks for A5U16, U19, and U22 are present, suspect A5U16, or U19, or U22.

8-269. If the preset number is present, check (while still looping on test) the $\overline{\text{N END}}$ signal at the output of A5U23. If this signal is not present and the clock is present at A5U15(4), then suspect one of the four N-counters. If the $\overline{\text{N END}}$ signal is present, follow it through U2B where it becomes $\overline{\text{S6}}$ which goes through A3U33 and A3U28 and becomes STB6 (status bit-6, N-measurements have been completed).

8-270. Test Section 16 (SERVICE REQUEST AND STATUS BYTE)

8-271. This section is testing the STATUS BYTE and the circuits responsible for supplying the data to the status register A3U33. The service request line is also checked for proper operation. The 5345A is programmed for FREQ A, EXTERNAL GATE, CHECK, and must function properly.

8-272. There are three tests in this section as shown in *Table 8-17*. The first two tests contain three subtests each. The third test has four subtests. The error printout message contains the test and subtest, numbers, the expected result (ER), and actual result (AR). ER and AR are octal representations of the STATUS BYTE.

8-273. The first test has three subtests. In the first subtest, the 9825A sends a reset (R) to the 5358A. The 5358A's status is read and all status bits should be inactive. In the second subtest, with the 5358A in the ACCUMULATE mode, the 9825A sends an initiate command (I). After 1-millisecond, the 5358A status is read. It should indicate a Service Request, N-measurements complete, and memory is not empty but less than half full. For subtest 3, status is immediately read again and all bits should be inactive because of the previous status read.

8-274. The second test also has three subtests. Status is read and all bits should be inactive because of the previous read in the first test. For the second subtest the 5358A is sent an initiate command (I) followed by a Halt (H). This causes a sync error because the 5358A is halted before it can complete it's "N" measurements. Status is read and should indicate this. For subtest 3, status is read again and all bits should be inactive because of the previous status read.

8-275. There are four tests in the third part. The first test is read status. All bits should be inactive. For the second test, the 5358A is sent an "I" (initiate) command. The 9825A then waits a length of time determined by the amount of memory in the 5358A. After the wait, the 9825A reads the status of the 5358A. Memory should be full, a Service Request should be present, and STB3 should be active indicating that an attempt was made to store data in memory when memory was full. Note that in this case when status is read, the status bits will be cleared if and only if the conditions which activated the bits are cleared before the status is read. Otherwise the bits will remain active. Because the conditions still exist, the 5358A is then sent an "R" (memory reset). Because STB4 and STB5 are the only two status bits which are not latched

they will be cleared indicating memory is empty. When status is read again, it should show a Service Request with an attempt to overrun memory and a sync error. Now, with the conditions no longer existing (memory empty), all the status bits should be cleared (because of the previous status read). This is what the fourth subtest checks. The 5358A status is read once more and all status bits should be inactive.

Table 8-17. Section 16 Tests

```
SEC 16
                16.1.1  ER=       0  AR=       0
                16.1.2  ER=     550  AR=     550
                16.1.3  ER=       0  AR=       0
                16.2.1  ER=       0  AR=       0
                16.2.2  ER=     502  AR=     502
                16.2.3  ER=       0  AR=       0
                16.3.1  ER=       0  AR=       0
                16.3.2  ER=     534  AR=     534
                16.3.3  ER=     106  AR=     106
                16.3.4  ER=       0  AR=       0
NO ERRORS - TEST COMPLETE
```

8-276. Troubleshooting Test Section 16

8-277. There are three tests in Section 16 and in each of these tests there are two subtests which check for exactly the same condition. In test one the subtests are one and three; in test two the subtests are one and three and in test three the subtests are one and four. Refer to *Table 8-17* and see that these six subtests are all checking for a STATUS BYTE of zero or in other words all status bits inactive. These conditions should exist because of previous status reads by the 9825A.

8-278. After status is read, the status latch A3U33 is sent a RESET pulse via A3U22C(10) which is a combination of the SERIAL POLL ENABLE signal needed to read status, and the DATA ACCEPT line at A3U36 (pins 12 and 11, respectively) which is part of the HP-IB handshake indicating that the STATUS BYTE has been accepted. Assuming all conditions which activated the latched Status Bits are clear before the Status Read, the Status Latch U33, should be cleared by this signal. By LOOPING ON FAILURE (key f_9) or by STOPPING ON FAILURE (key f_8) the fault can be located with a logic probe or scope by first looking for the reset pulse A3U22C(10). If this is present, examine the bit inputs of the latch (U33) and determine which bits are not being cleared.

8-279. As shown in *Table 8-17* there are four subtests in which the 9825A reads Status and expects a value other than zero. By converting the ER and AR from the error printout into binary form, the active bits will be indicated. By using either STOP ON FAILURE f_8 or LOOP ON FAILURE f_9 keys, the faulty bit line can be traced.

8-280. Test Section 17 (DEAD TIME)

8-281. Up through Section 16, all testing of the 5358A is done in the minimum dead time (DØK) mode. Section 17 checks the other three dead time modes which are ratio 1:1 (D1K), ratio 2:1 (D2K), and external (D3K). The 5345A is programmed for FREQ A, MIN GATE TIME, CHECK and must function properly.

8-282. Section 17 contains four tests. Each test programs and checks each of the four dead time modes in numeric order (test 1 for DØK through test 4 for D3K). The 5358A is programmed to make 10 measurements (N10) with the measurement time of 10 milliseconds (M1E4K) and a transfer of 1-digit (T1).

8-283. The first test programs the 5358A for the minimum dead time mode (DØK). An "I" is sent to the 5358A to initiate the measurements. After 78 milliseconds the status of the 5358A is read. The STATUS BYTE should indicate a Service Request indicating memory is not empty and "N" measurements are complete (150 in octal). The two STATUS BYTES are put into octal form and compared to the expected value. A mismatch constitutes an error condition and is indicated by the error printout.

8-284. The second test programs the 5358A for the ratio 1:1 (D1K) mode. An "I" is sent and the status is checked as in test 1 except that the 9825A waits 126 milliseconds before the first status reading.

8-285. The third test programs the 5358A for the ratio 2:1 (D2K) mode. An "I" is sent and the status is checked as in test 1 except the 9825A waits 126 milliseconds before the first status reading.

Table 8-18. Section 17 Tests

17.1	ER=	10150	AR=	10150
17.2	ER=	10150	AR=	10150
17.3	ER=	10150	AR=	10150
17.4	ER=	10010	AR=	10010

8-286. The fourth test in this section program the 5358A for the External dead time (D3K) mode. An "I" is sent and the status is checked in the same way as in the previous tests except the 9825A waits 174 milliseconds before taking the first status reading. With no external trigger to stop the dead time after the first measurement, the 5358A will remain in the dead time (non-measurement) state. Because of this, status of the 5358A will be the same for both readings (010 octal) indicating that memory is not empty but less than half full. This status indicates that one measurement was made and transferred to the 5358A.

8-287. Troubleshooting Test Section 17

8-288. LOOP ON FAILURE f_9 or STOP ON FAILURE f_8 is effective. Depending on which of the four tests fail, verify that the correct Dead Time mode has been selected by checking the outputs of A6U16. If they are incorrect, check the two input selector lines of U16 (U16(1) and U16(2)). If they are incorrect, loop on failure and check for the presence of a clock on pin line of A6U17(9). If the clock is present and the clear (pin 1) is high, suspect U17.

8-289. SCHEMATIC DIAGRAMS

8-290. Schematic diagrams, including component locators, are included for each assembly as follows:

Figure 8-7 A3 HP-IB Control Assembly
Figure 8-8 A4 Memory Control Assembly
Figure 8-9 A5 System Control Assembly
Figure 8-10 A6 Gate Control Assembly
Figure 8-11 A7 Converter Assembly
Figure 8-12 A8 Memory Assembly
Figure 8-13 A12 Display Assembly and A13 BNC I/O Assembly

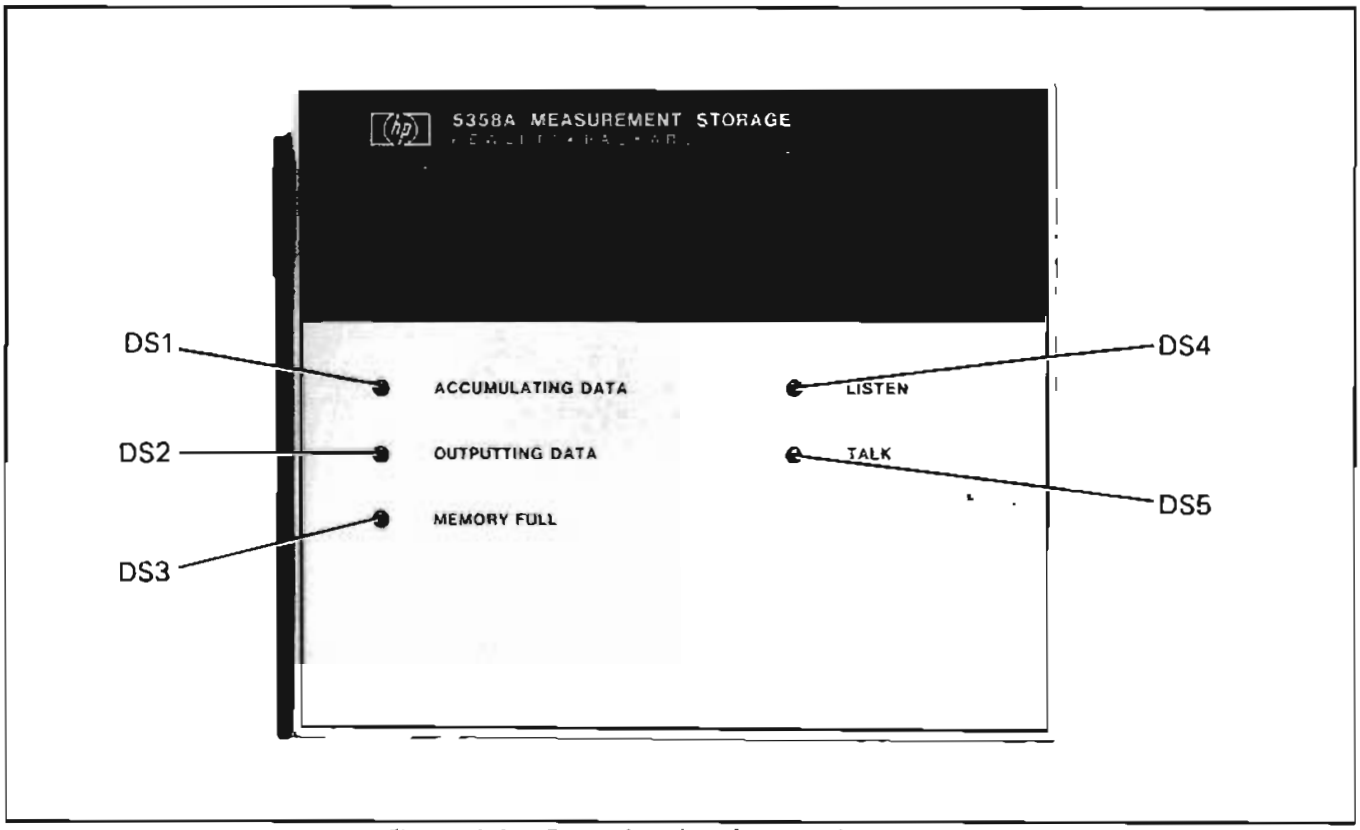


Figure 8-3. Front Panel Reference Designators

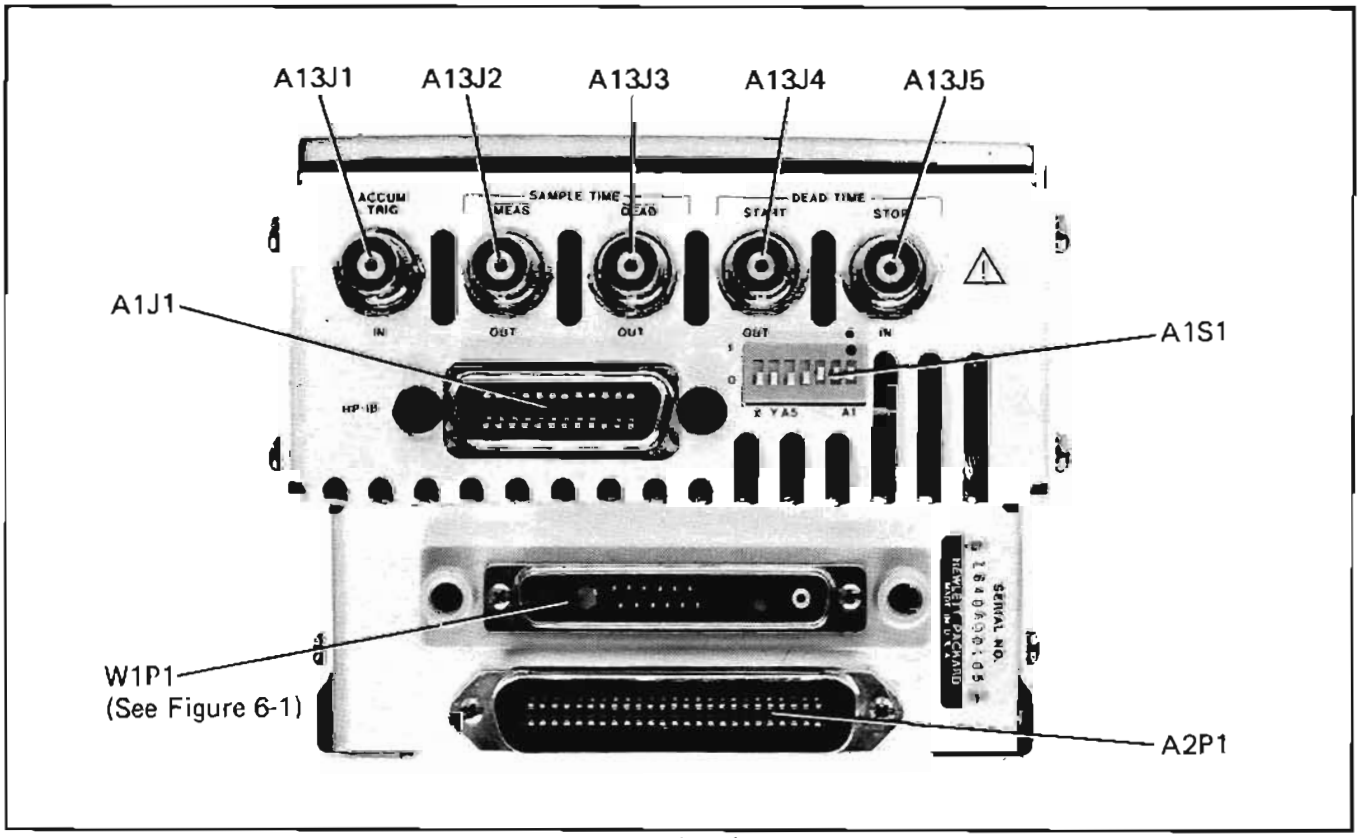


Figure 8-4. Rear Panel Reference Designators

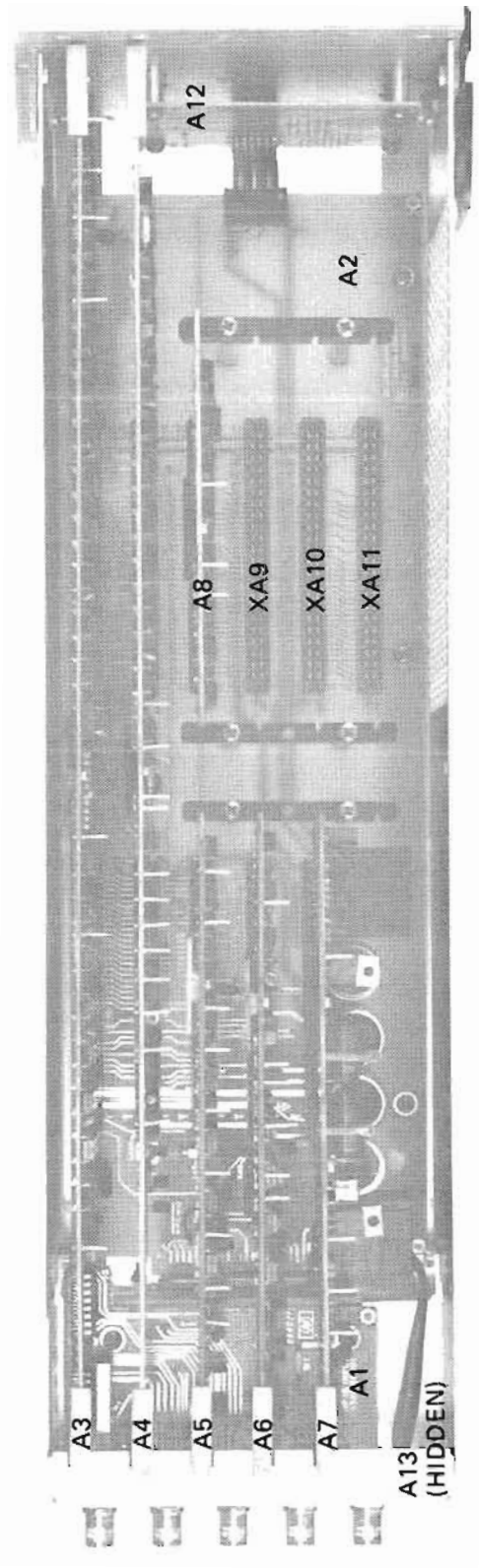


Figure 8-5. Assembly Locations

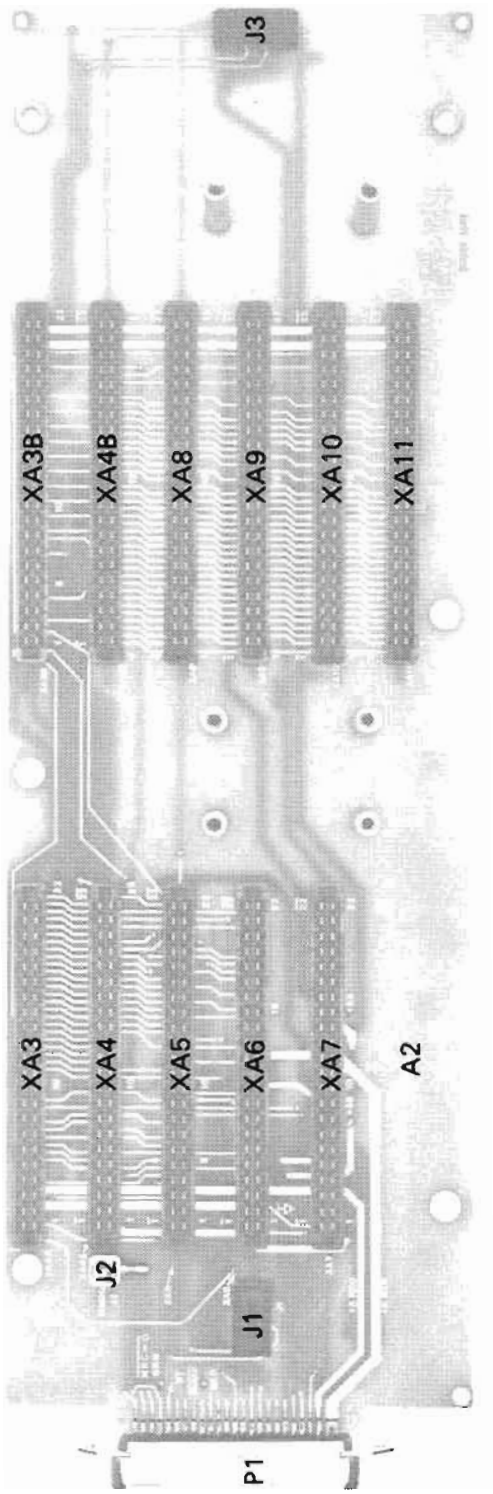
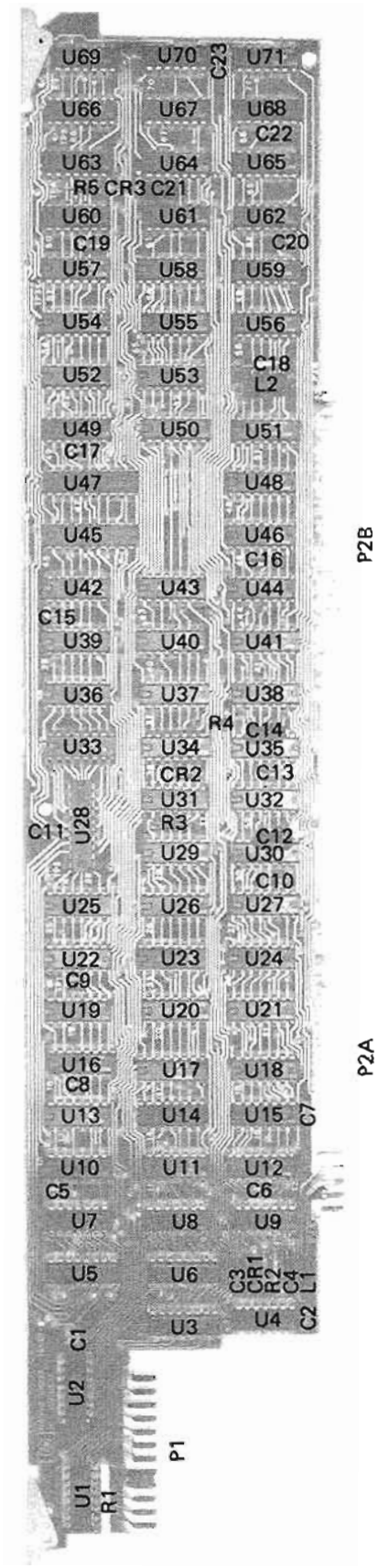
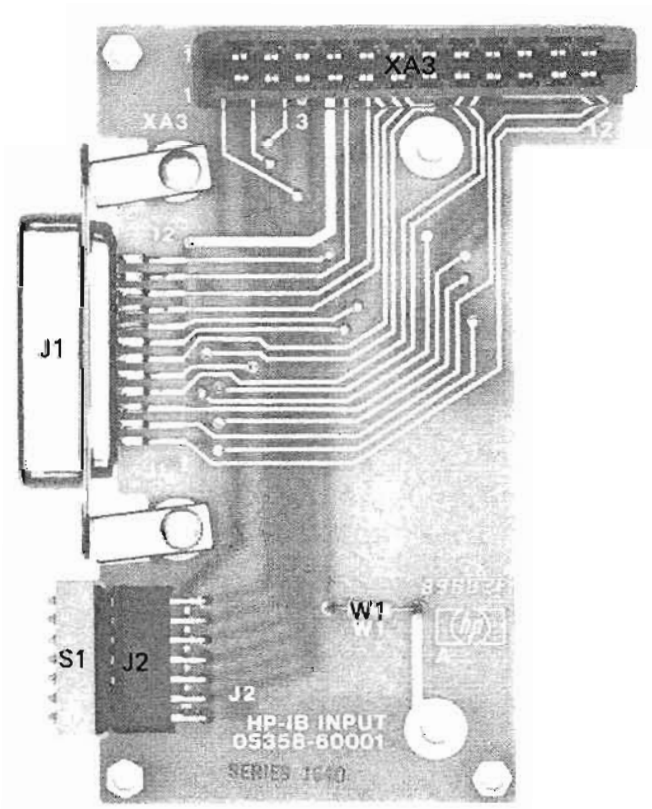


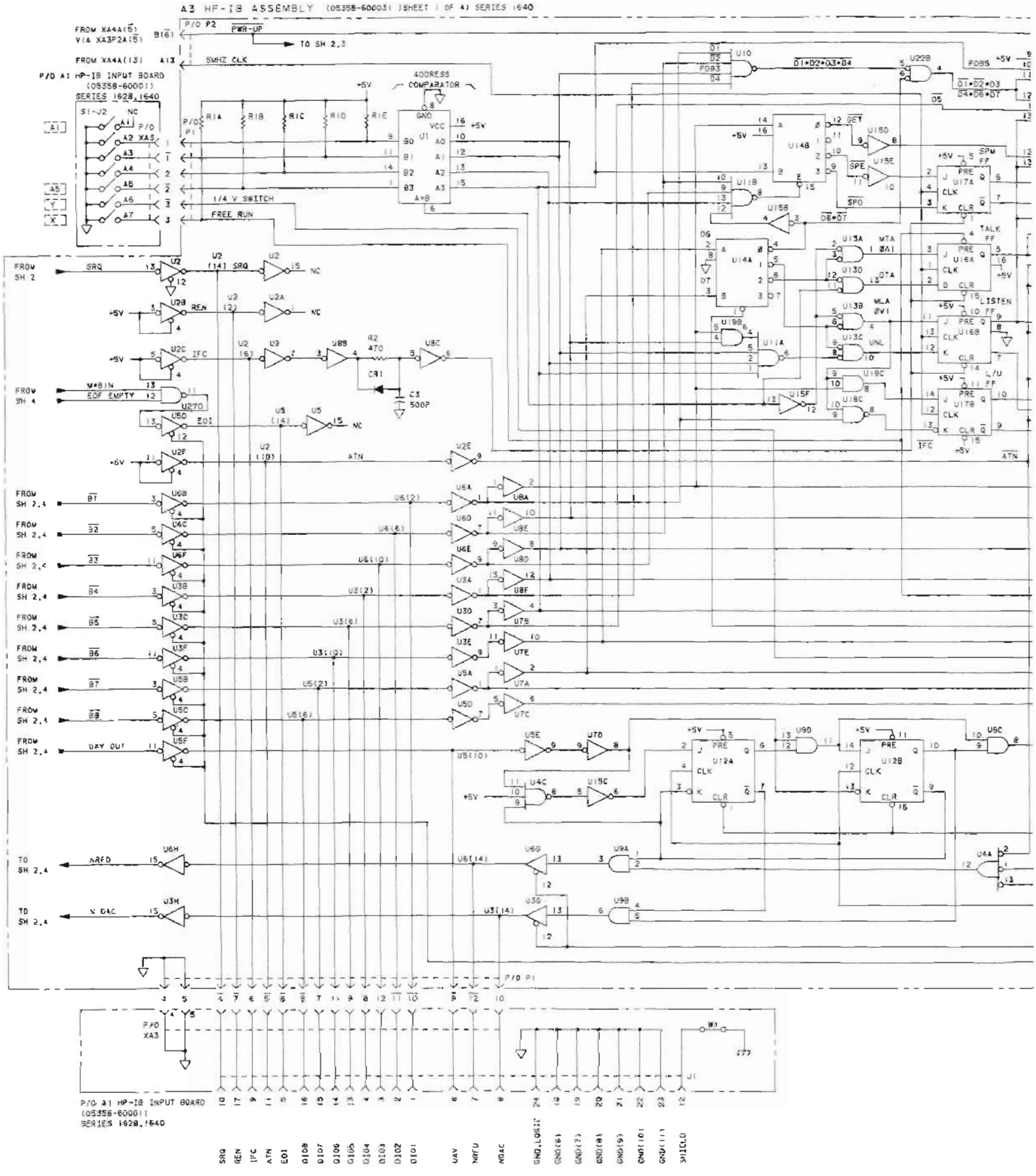
Figure 8–6. A2 Motherboard Reference Designations

A3


U69
U70
C23
U71
U66
U67
U68
C22
U63
U64
U65
R6 CR3 C21
U60
U61
U62
C19
C20
U57
U58
U59
U54
U55
U56
C18
U52
U53
L2
U49
U50
U51
C17
U47
U48
U45
U46
C16
P2B
U42
U43
U44
C15
U39
U40
U41
U36
U37
U38
R4
C14
U33
U34
U35
CR2
C13
U31
U32
C11
U28
R3
C12
U29
U30
C10
U25
U26
U27
U22
U23
U24
C9
U19
U20
U21
P2A
U16
U17
U18
C8
U13
U14
U15
C7
U10
U11
U12
C5
C6
U7
U8
U9
U5
U6
C3
CR1
R2
C4
L1
U3
U4
C2
C1
U2
P1
U1
R1

A1


XA3
XA3
J1
W1
S1
J2
J2
HP-IB INPUT
05358-60001


A3 HP-IB ASSEMBLY (05358-60003) SHEET 1 OF 4) SERIES 1640
P/O A1 HP-IB INPUT BOARD (05358-60001) SERIES 1628, 1640
ADDRESS COMPARATOR
1/4 V SWITCH
FREE RUN
SMHZ CLK
PWR-UP
TO SH 2,3
SRQ
REN
IFC
ATN
EOI
DAV
NRFD
NDAC
TALK FF
LISTEN FF
SPM FF
L/U FF
P/O P1
P/O XA3
P/O A1 HP-IB INPUT BOARD (05358-60001) SERIES 1628, 1640
SRQ REN IFC ATN EOI D108 D107 D106 D105 D104 D103 D102 D101 DAV NRFD NDAC GND,LOGIC GND(6) GND(7) GND(8) GND(9) GND(10) GND(11) SHIELD

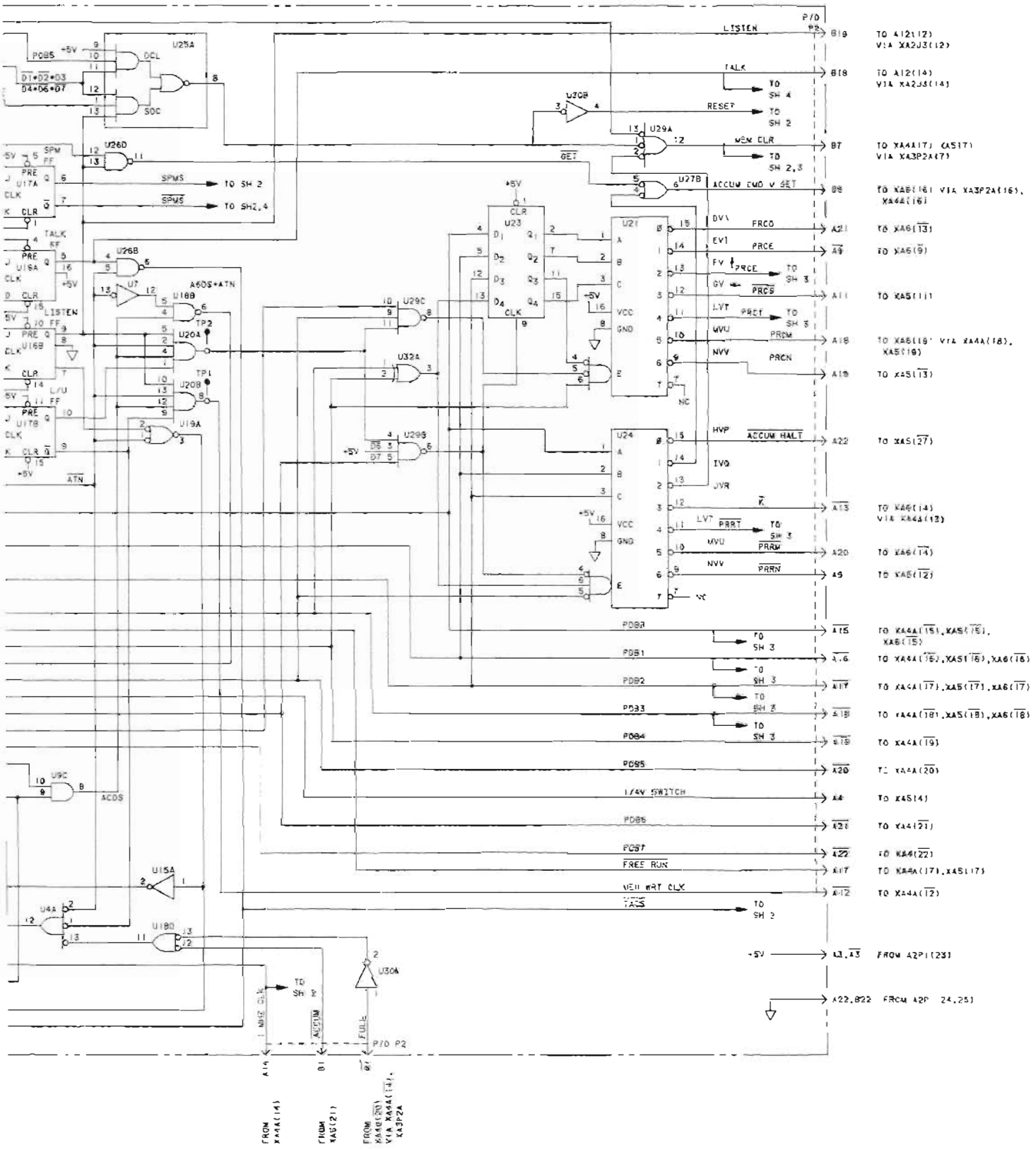
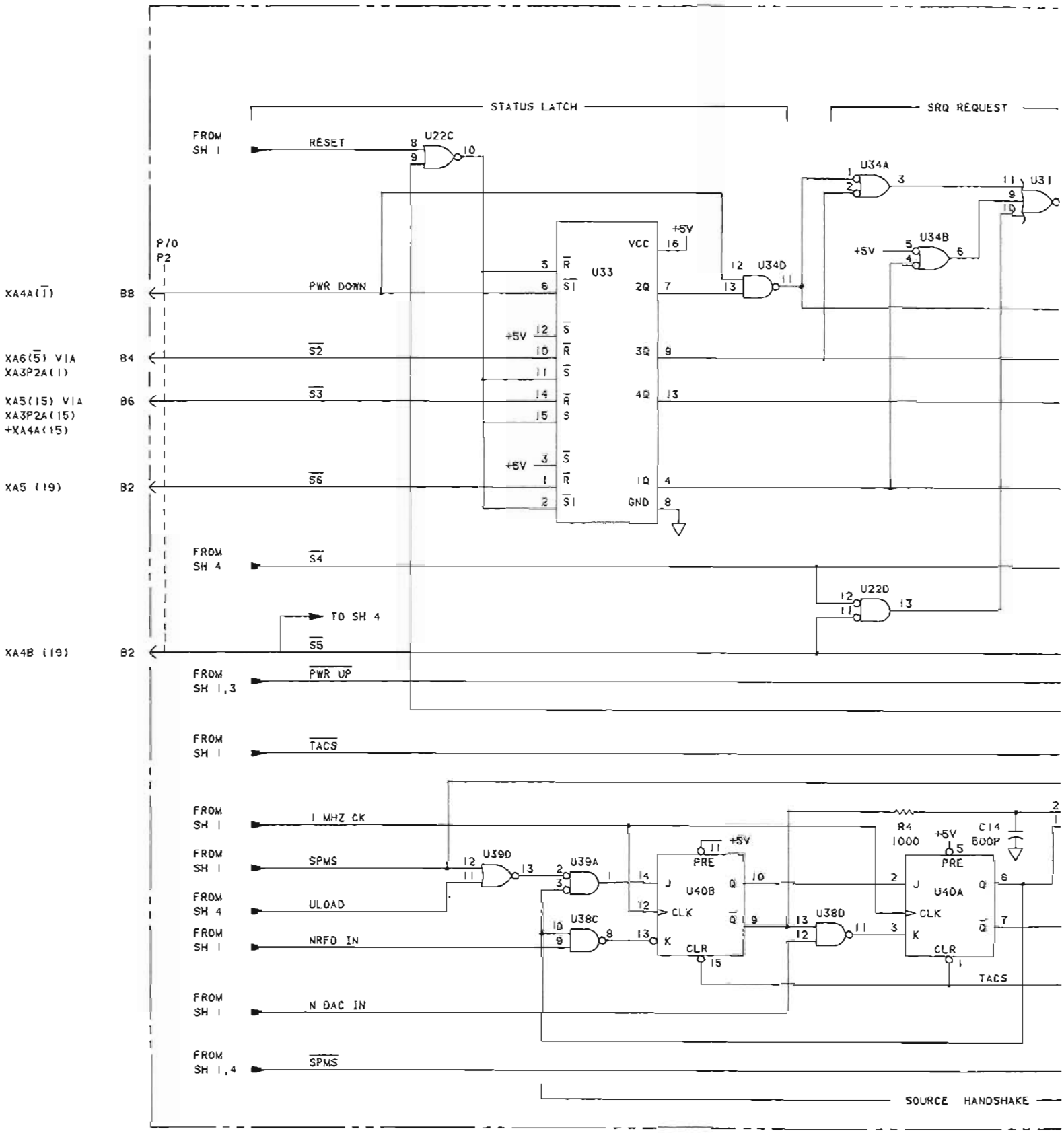


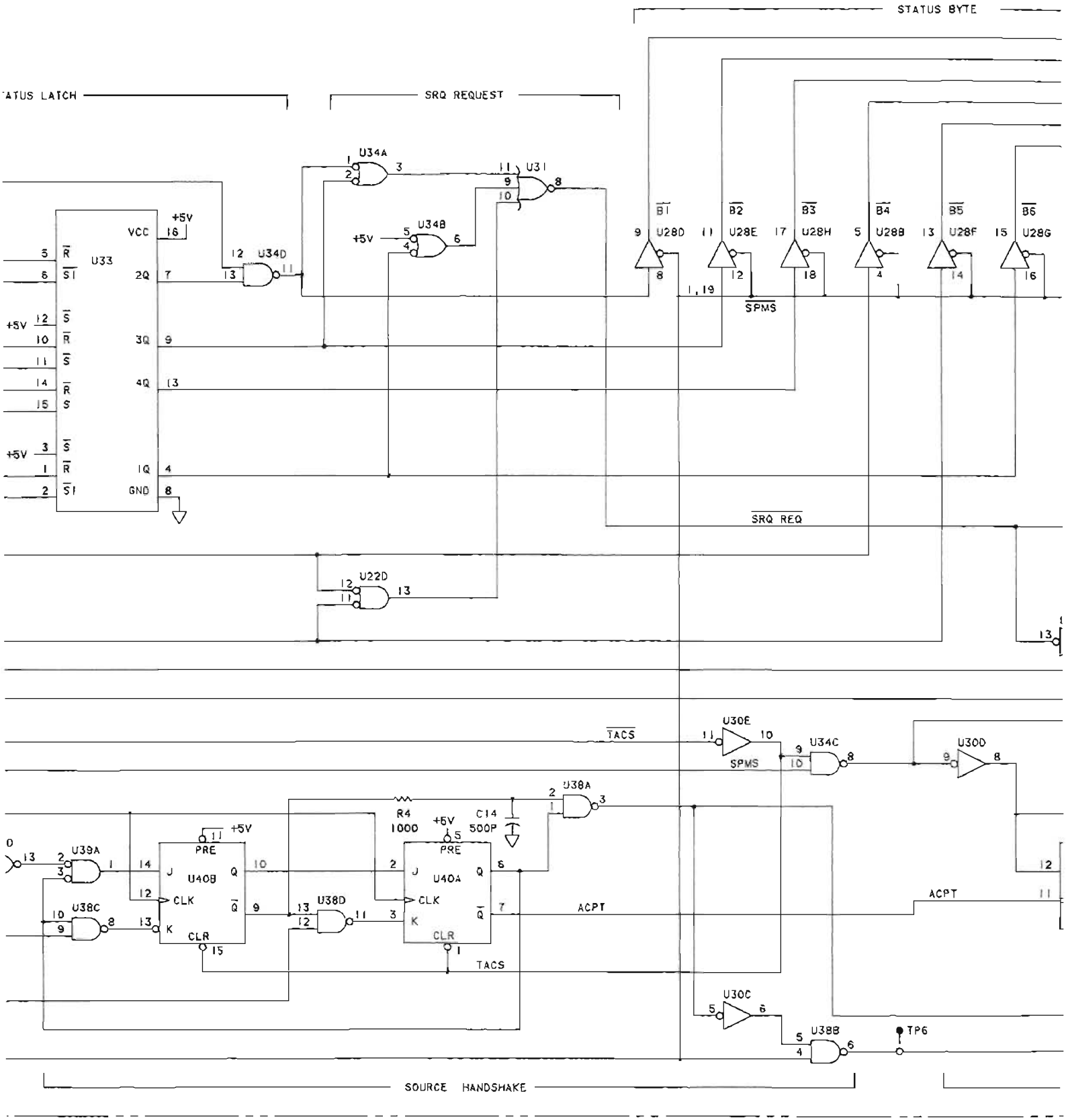
Figure 8-7. A1 HP-IB Input Assembly and A3 HP-IB Control Assembly (Sheet 1 of 4)

Figure 8-7
A1 HP-IB INPUT ASSEMBLY AND
A3 HP-IB CONTROL ASSEMBLY
(Sheet 1 of 4)

(See Page 8–45)

A3 HP-IB ASSEMBLY (05358-60003)(SHEET 2 OF 4) SERIES 1640




STATUS BYTE
ATUS LATCH
SRQ REQUEST
U33
VCC
GND
+5V
U34A
U34B
U34D
U31
U28D
U28E
U28H
U28B
U28F
U28G
B1
B2
B3
B4
B5
B6
SPMS
SRQ REQ
U22D
TACS
U30E
U34C
U30D
U38A
R4
1000
C14
500P
U39A
U38C
U40B
U40A
U38D
PRE
CLR
CLK
ACPT
U30C
U38B
TP6
SOURCE HANDSHAKE

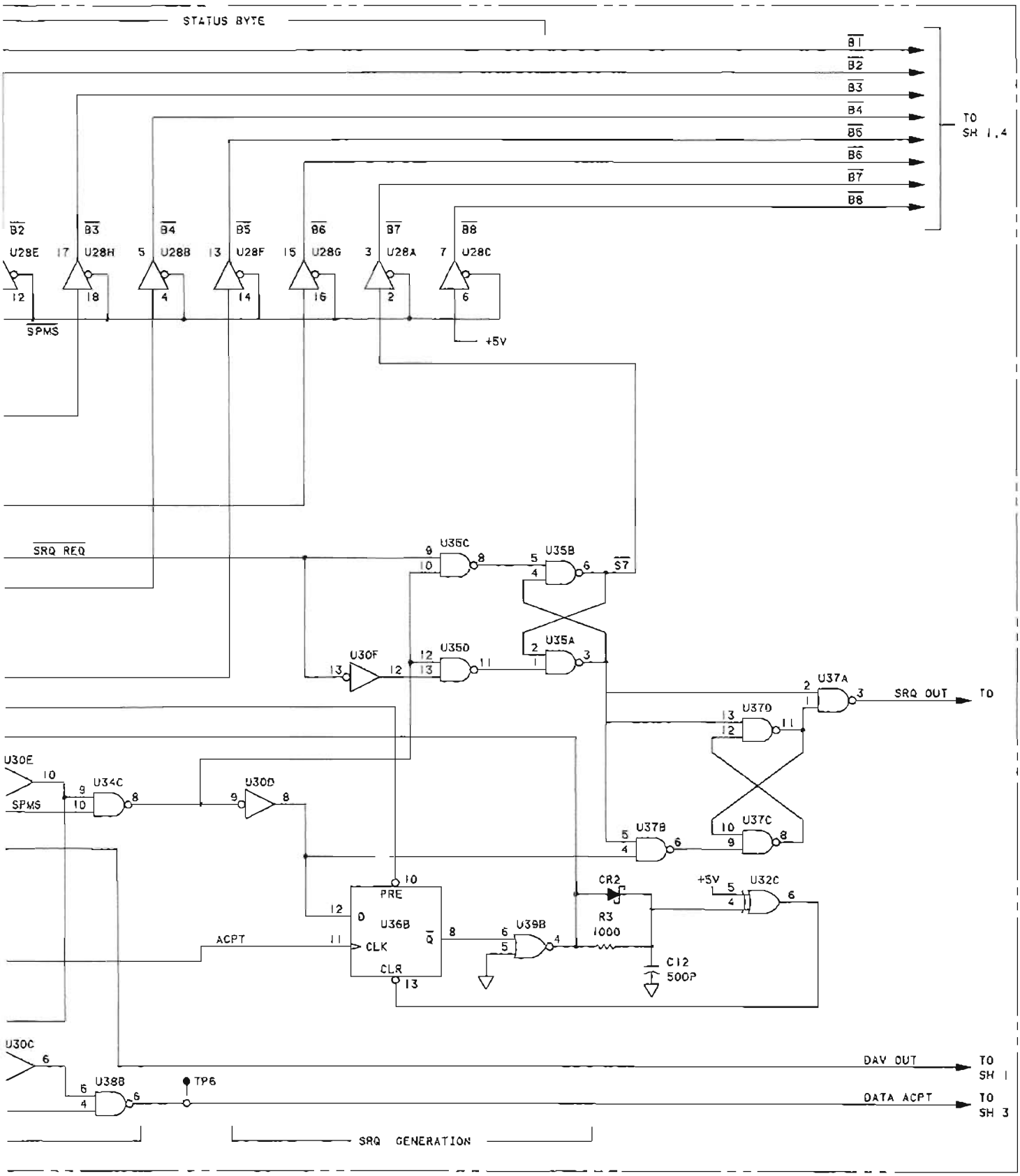
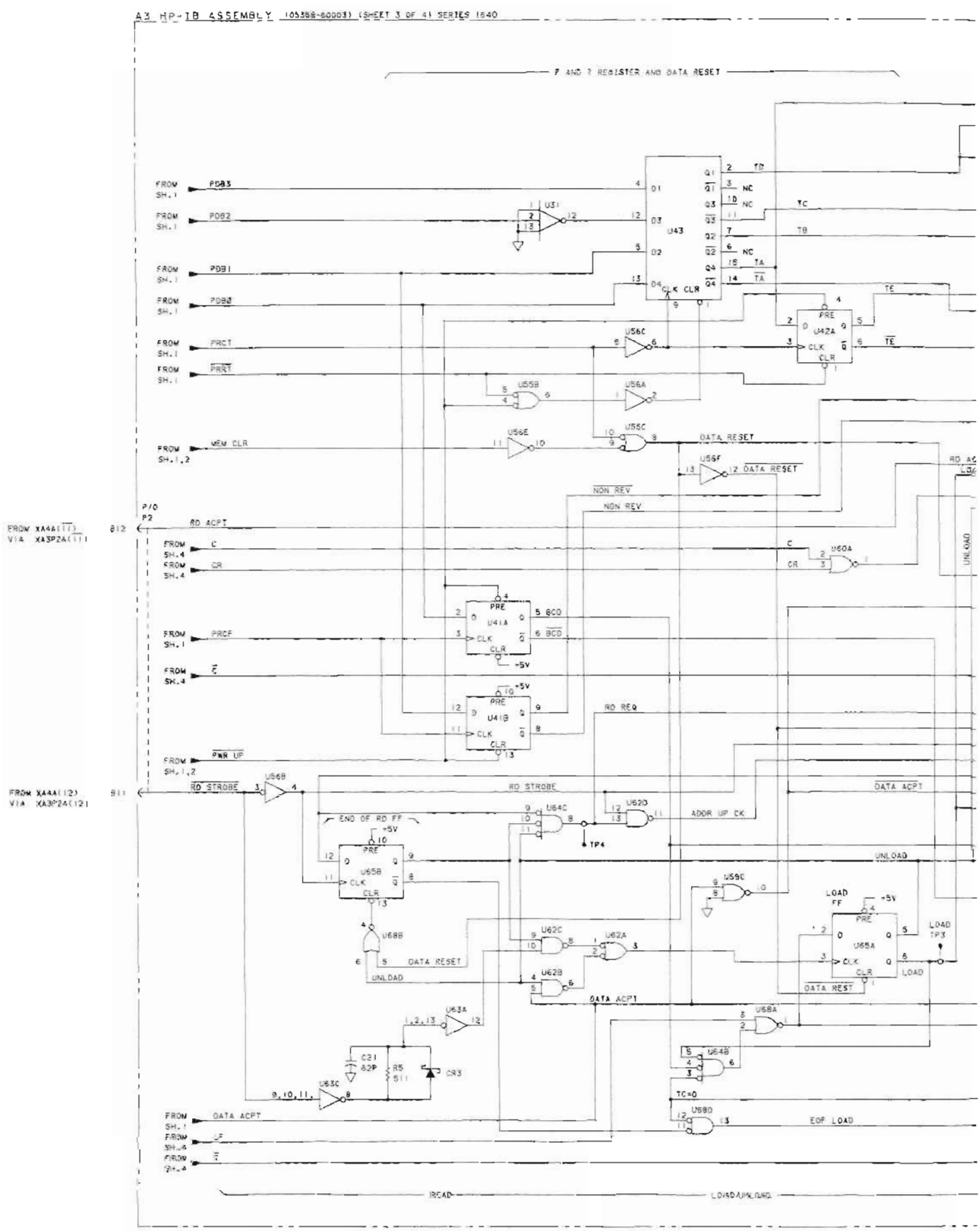


Figure 8-7. A1 HP-IB Input Assembly and A3 HP-IB Control Assembly
(Sheet 2 of 4)

Figure 8-7
A1 HP-IB INPUT ASSEMBLY AND
A3 HP-IB CONTROL ASSEMBLY
(Sheet 2 of 4)

(See Page 8-47)

A3 HP-IB ASSEMBLY 05359-60003 (SHEET 3 OF 4) SERIES 1640



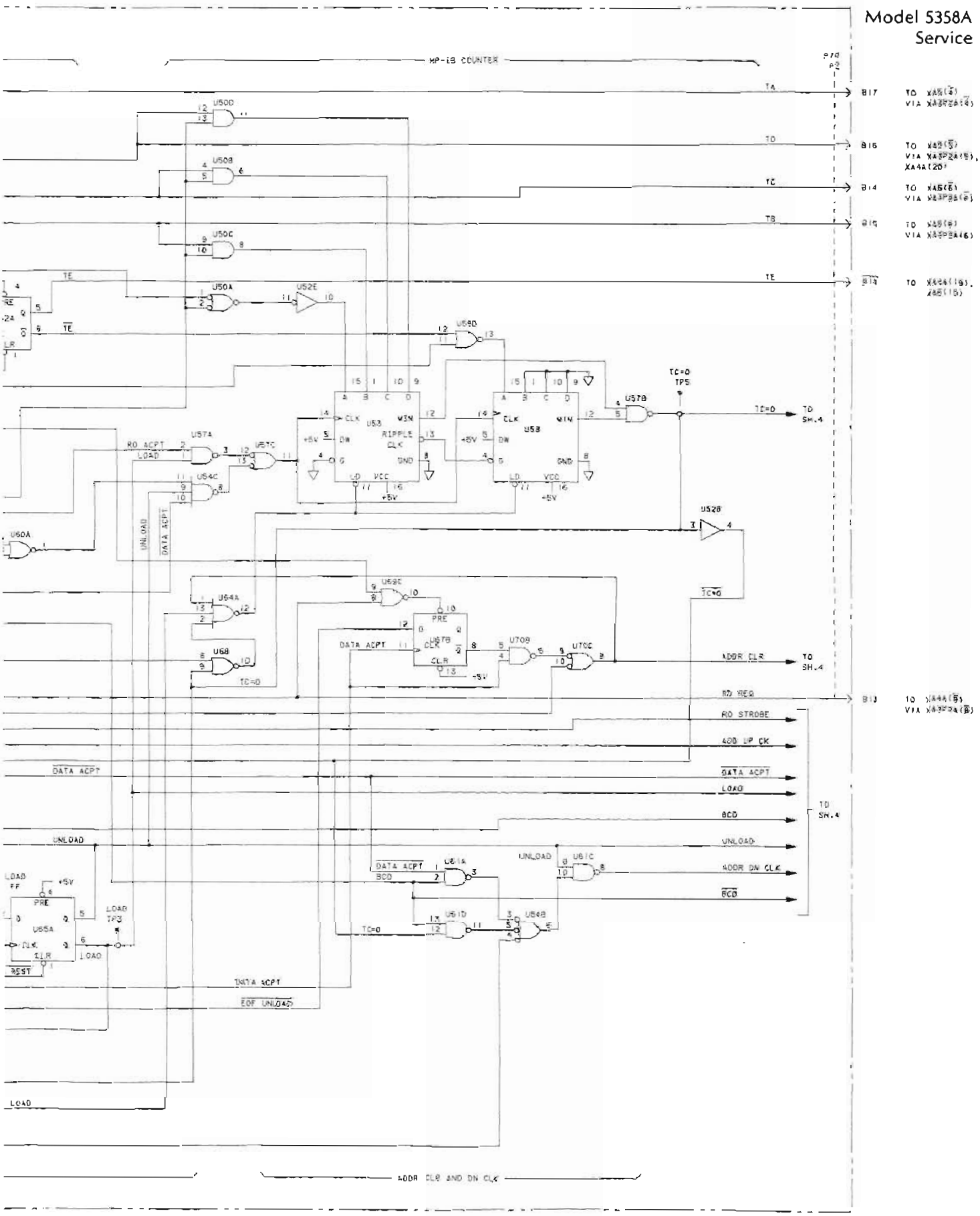
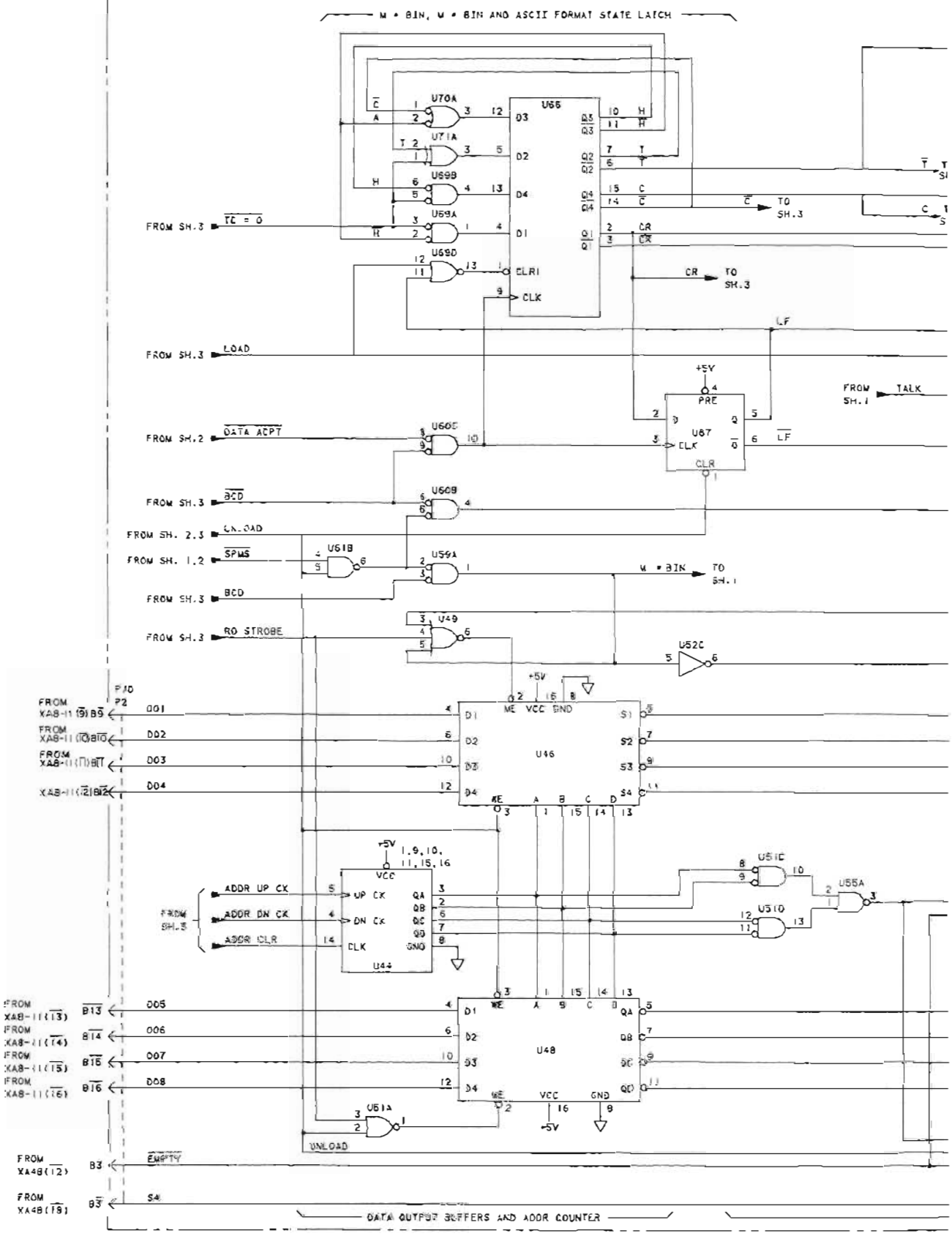


Figure 8–7. A1 HP-IB Input Assembly and A3 HP-IB Control Assembly (Sheet 3 of 4)

Figure 8-7
A1 HP-IB INPUT ASSEMBLY AND
A3 HP-IB CONTROL ASSEMBLY
(Sheet 3 of 4)

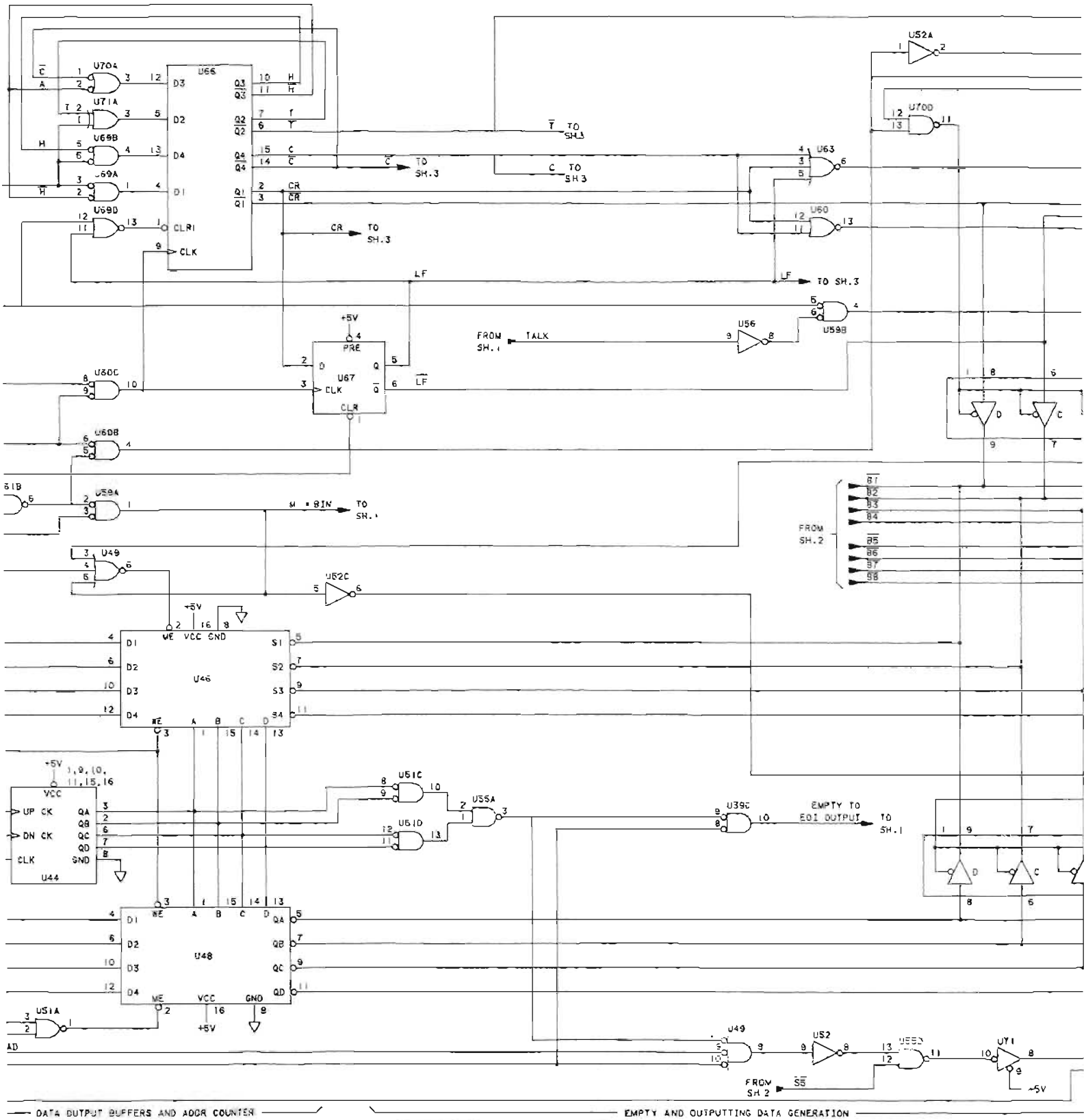
(See Page 8-49)

A3 HP-IB ASSEMBLY (08368-60003) (SHEET 4 OF 4) SERIES 1640



M = BIN, M = BIN AND ASCII FORMAT STATE LATCH

BCD1, BCD2, C,



DATA OUTPUT BUFFERS AND ADDR COUNTER

EMPTY AND OUTPUTTING DATA GENERATION

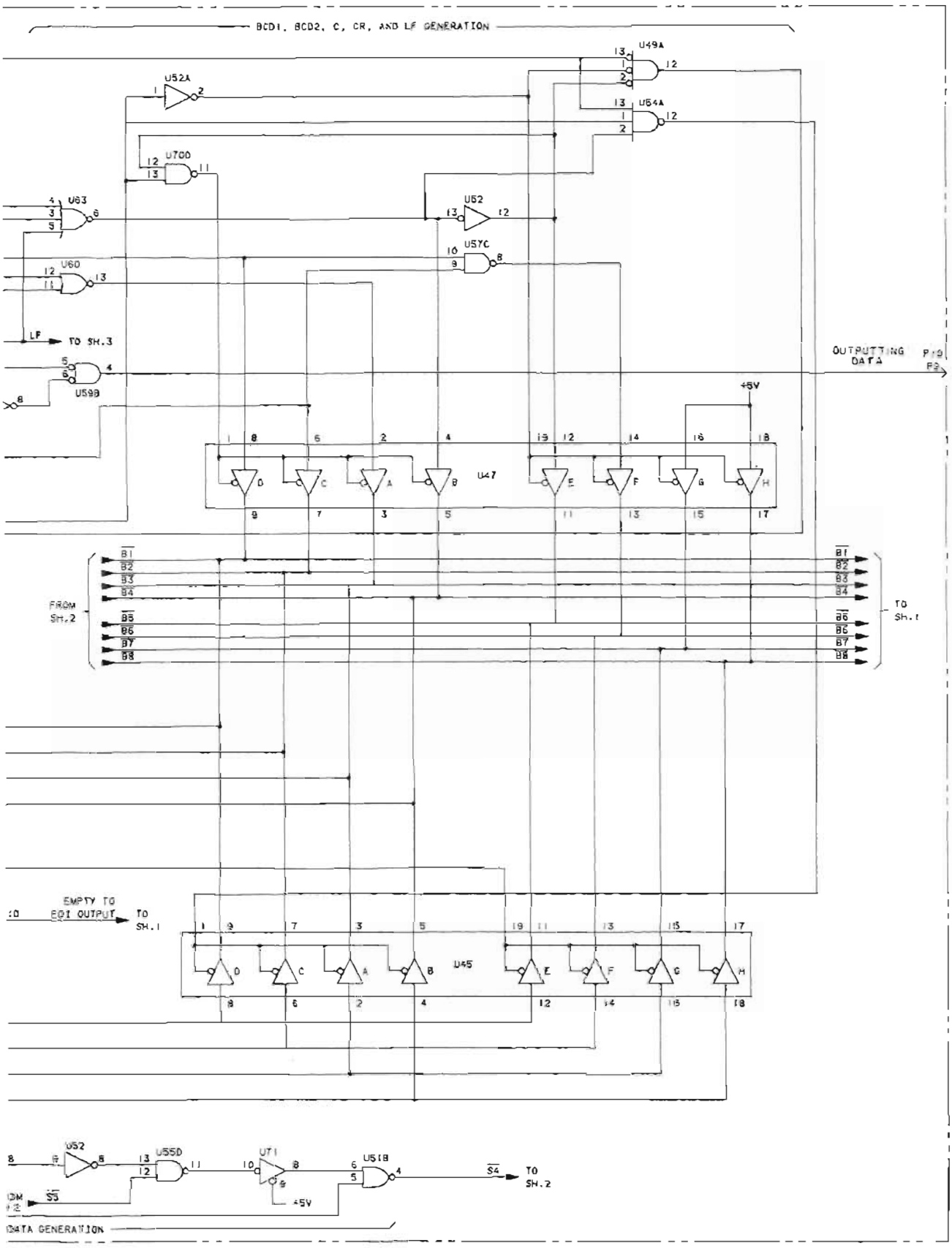
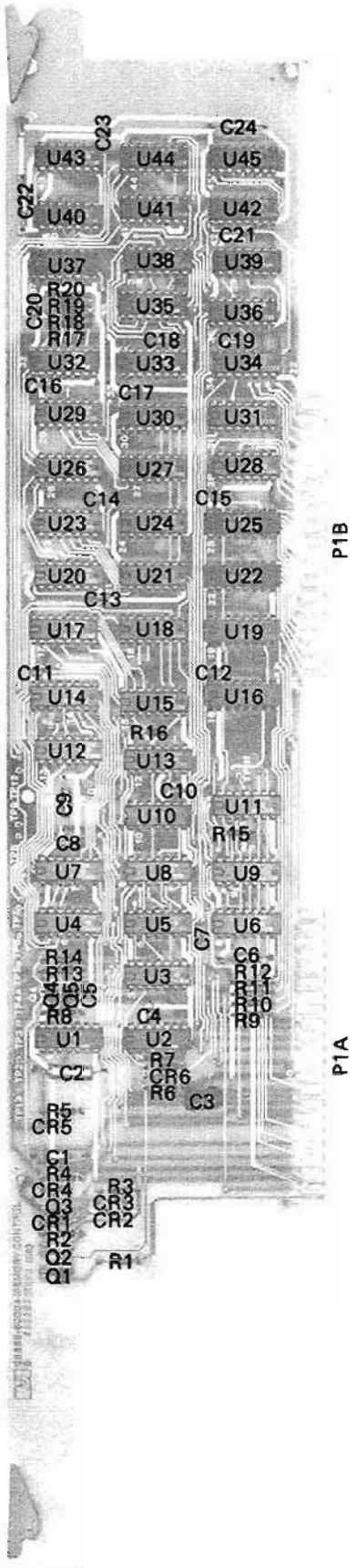


Figure 8-7. A1 HP-IB Input Assembly and A3 HP-IB Control Assembly
(Sheet 4 of 4)

Figure 8-7
A1 HP-IB INPUT ASSEMBLY AND
A3 HP-IB CONTROL ASSEMBLY
(Sheet 4 of 4)

(See Page 8-51)


C23
C24
U43
U44
U45
C22
U40
U41
U42
C21
U37
U38
U39
R20
R19
R18
C20
U35
U36
R17
C18
C19
U32
U33
U34
C16
C17
U29
U30
U31
U26
U27
U28
C14
C15
U23
U24
U25
P1B
U20
U21
U22
C13
U17
U18
U19
C11
C12
U14
U15
U16
R16
U12
U13
C10
C9
U10
U11
R15
C8
U7
U8
U9
U4
U5
C7
U6
R14
C6
R13
U3
R12
C5
R11
R8
C4
R10
R9
U1
U2
P1A
R7
C2
CR6
R6
C3
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C1
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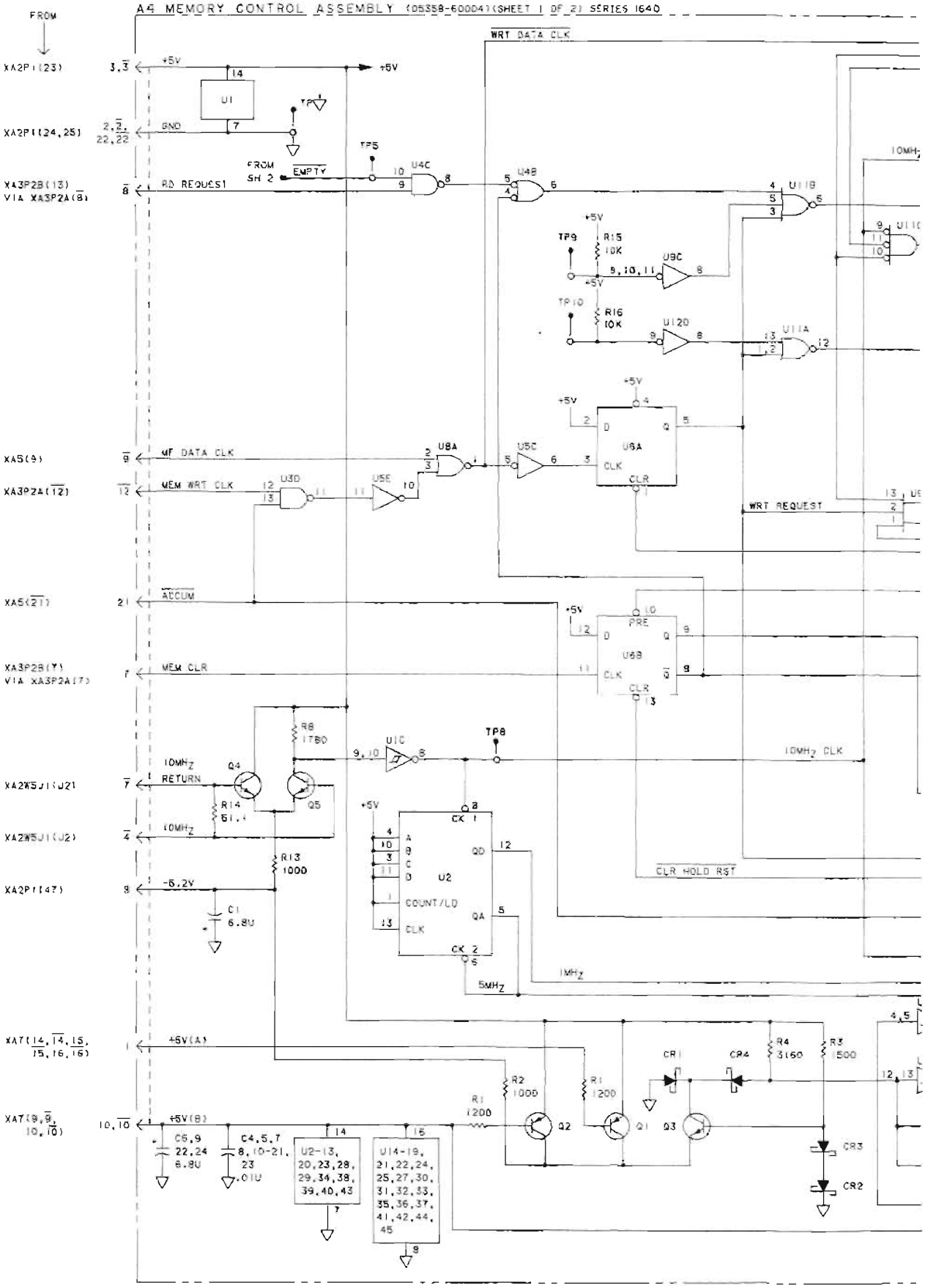
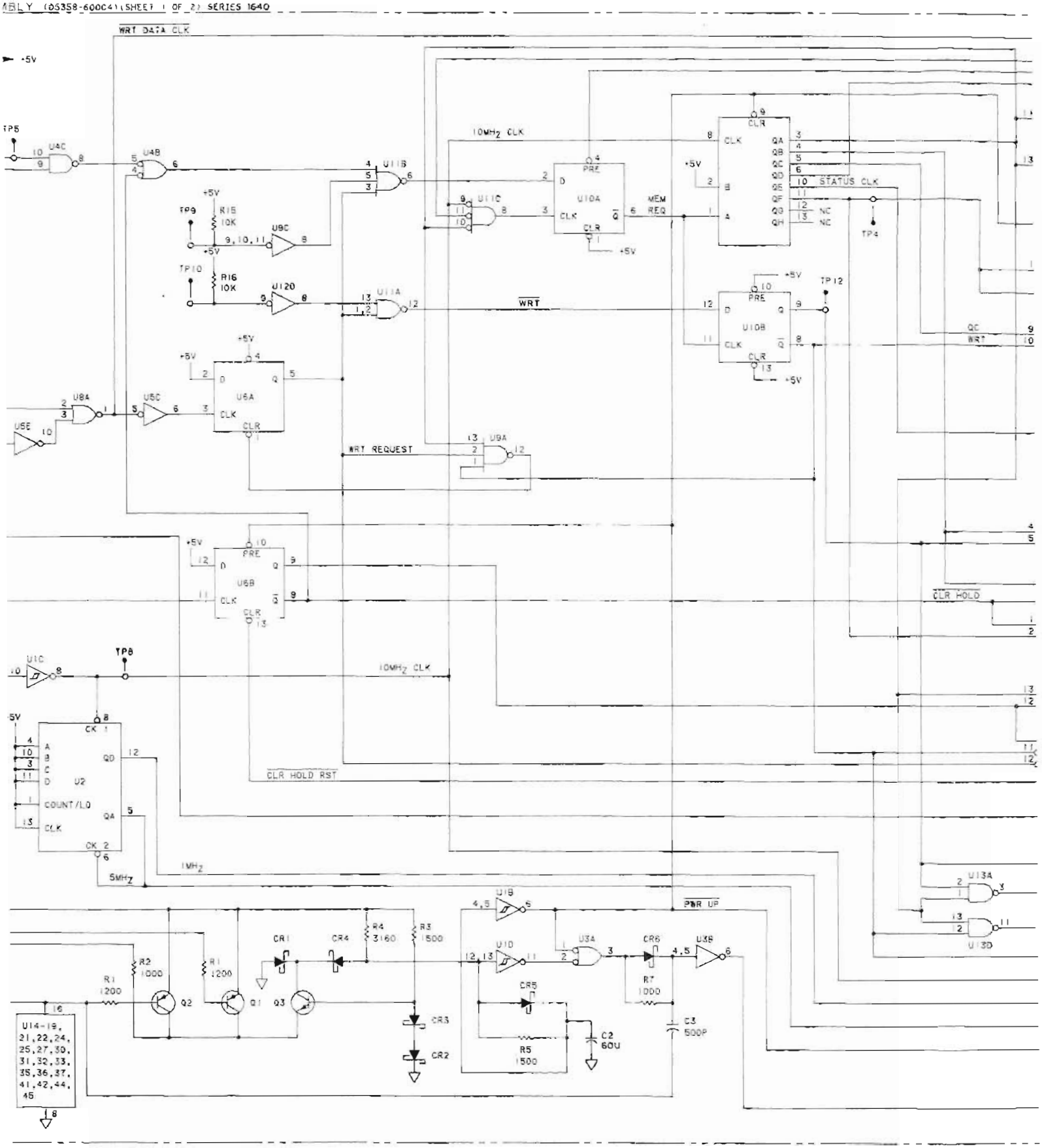
R3
Q3
CR3
CR1
CR2
R2
Q2
R1
Q1


A4 MEMORY CONTROL ASSEMBLY (05358-60004) (SHEET 1 OF 2) SERIES 1640
FROM
XA2P1(23)
XA2P1(24,25)
XA3P2B(13) VIA XA3P2A(8)
XA5(9)
XA3P2A(12)
XA5(21)
XA3P2B(7) VIA XA3P2A(7)
XA2W5J1(J21)
XA2W5J1(J2)
XA2P1(47)
XA7(14,14,15,15,16,16)
XA7(9,9,10,10)
WRT DATA CLK
RD REQUEST
MF DATA CLK
MEM WRT CLK
ACCUM
MEM CLR
10MHz RETURN
10MHz
-5.2V
+5V(A)
+5V(B)
GND
FROM SH 2
EMPTY
WRT REQUEST
10MHz CLK
CLR HOLD RST
1MHz
5MHz
U1
U2
U3D
U4B
U4C
U5C
U5E
U6A
U6B
U8A
U8C
U10B
U10C
U11A
U12D
TP5
TP6
TP8
TP9
TP10
R1 1200
R2 1000
R3 1500
R4 3160
R5 1000
R6 1780
R13 1000
R14 61.9
R15 10K
R16 10K
C1 6.8U
C6,9 22,24 6.8U
C4,5,7 8,10-21, 23 .01U
U2-13, 20,23,28, 29,34,38, 39,40,43
U14-19, 21,22,24, 25,27,30, 31,32,33, 35,36,37, 41,42,44, 45
Q1
Q2
Q3
Q4
Q5
CR1
CR2
CR3
CR4


WRT DATA CLK
+5V
TP5
U4C
U4B
U11B
10MHz CLK
U11C
U10A
MEM REQ
STATUS CLK
TP4
TP9
R15 10K
U9C
TP10
R16 10K
U12D
U11A
WRT
TP12
U10B
QC WRT
U8A
U8C
U8E
U6A
WRT REQUEST
U9A
U8B
CLR HOLD
TP8
U1C
CLR HOLD RST
U2
COUNT/LD
1MHz
5MHz
U1B
PWR UP
U3A
U1D
U3B
U13A
U13D
CR1
CR4
R4 3160
R3 1500
R2 1000
R1 1200
Q2
Q1
Q3
CR3
CR2
CR5
R5 1500
C2 60U
CR6
R7 1000
C3 500P
U14-19, 21,22,24, 25,27,30, 31,32,33, 35,36,37, 41,42,44, 45

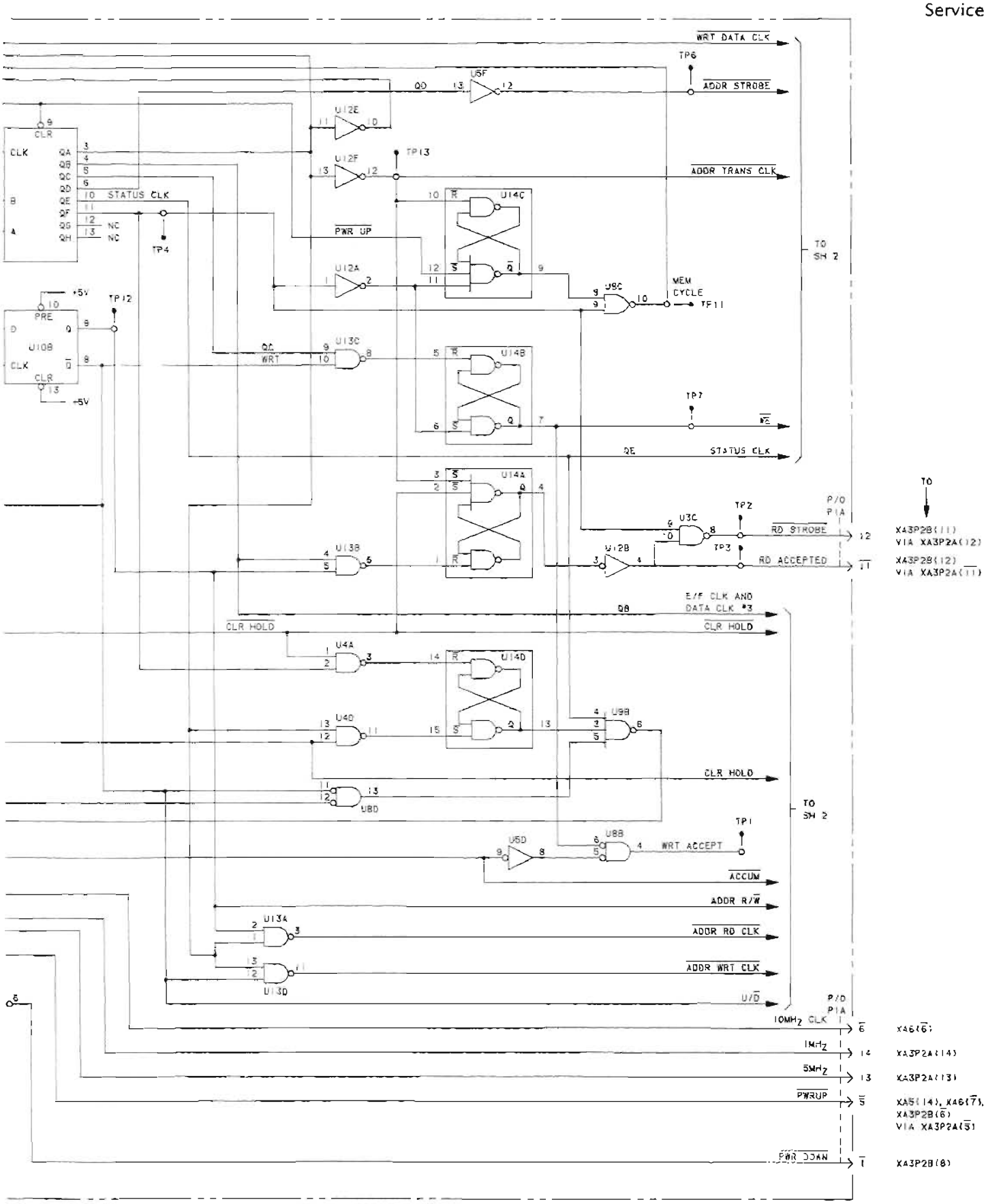
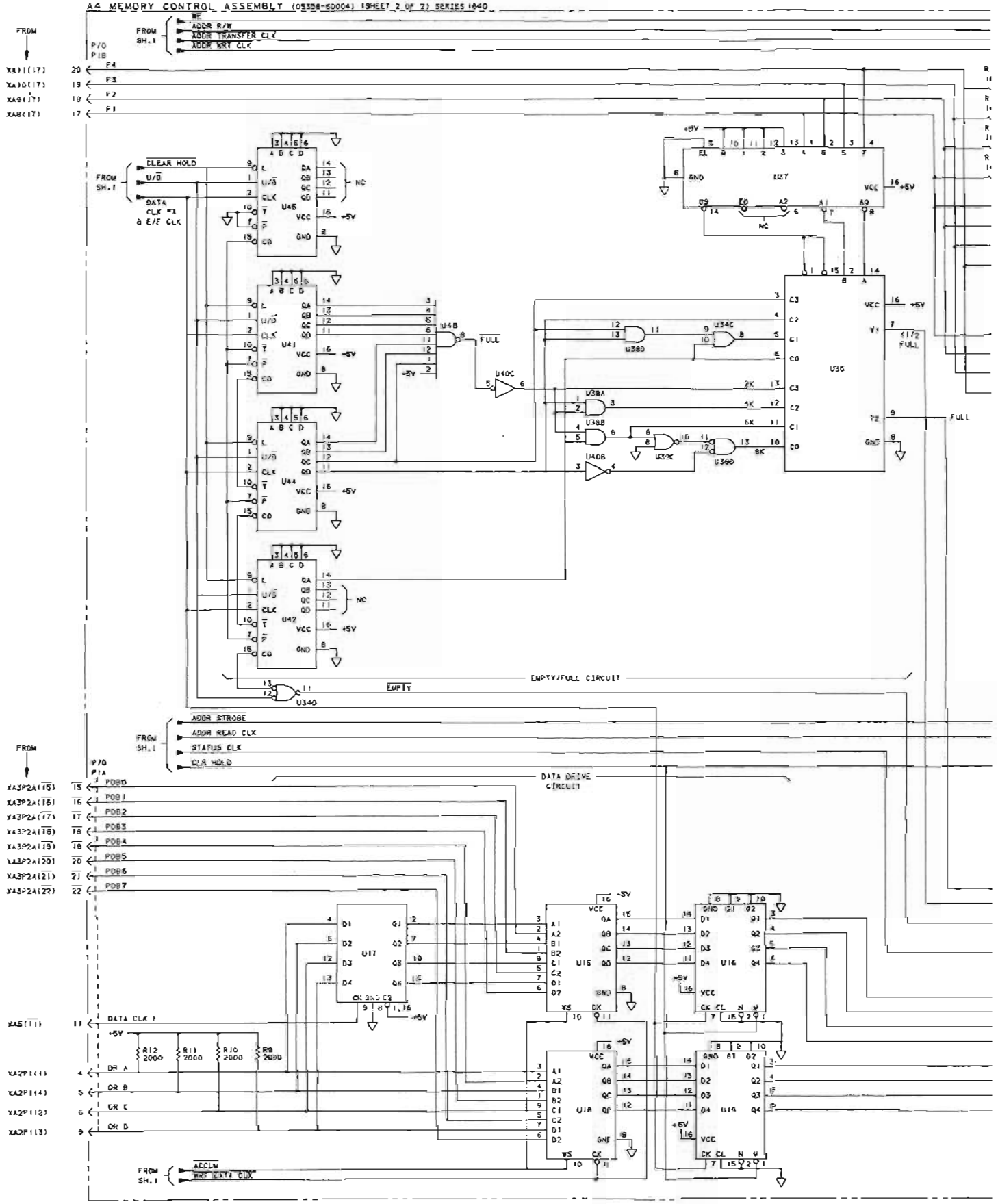


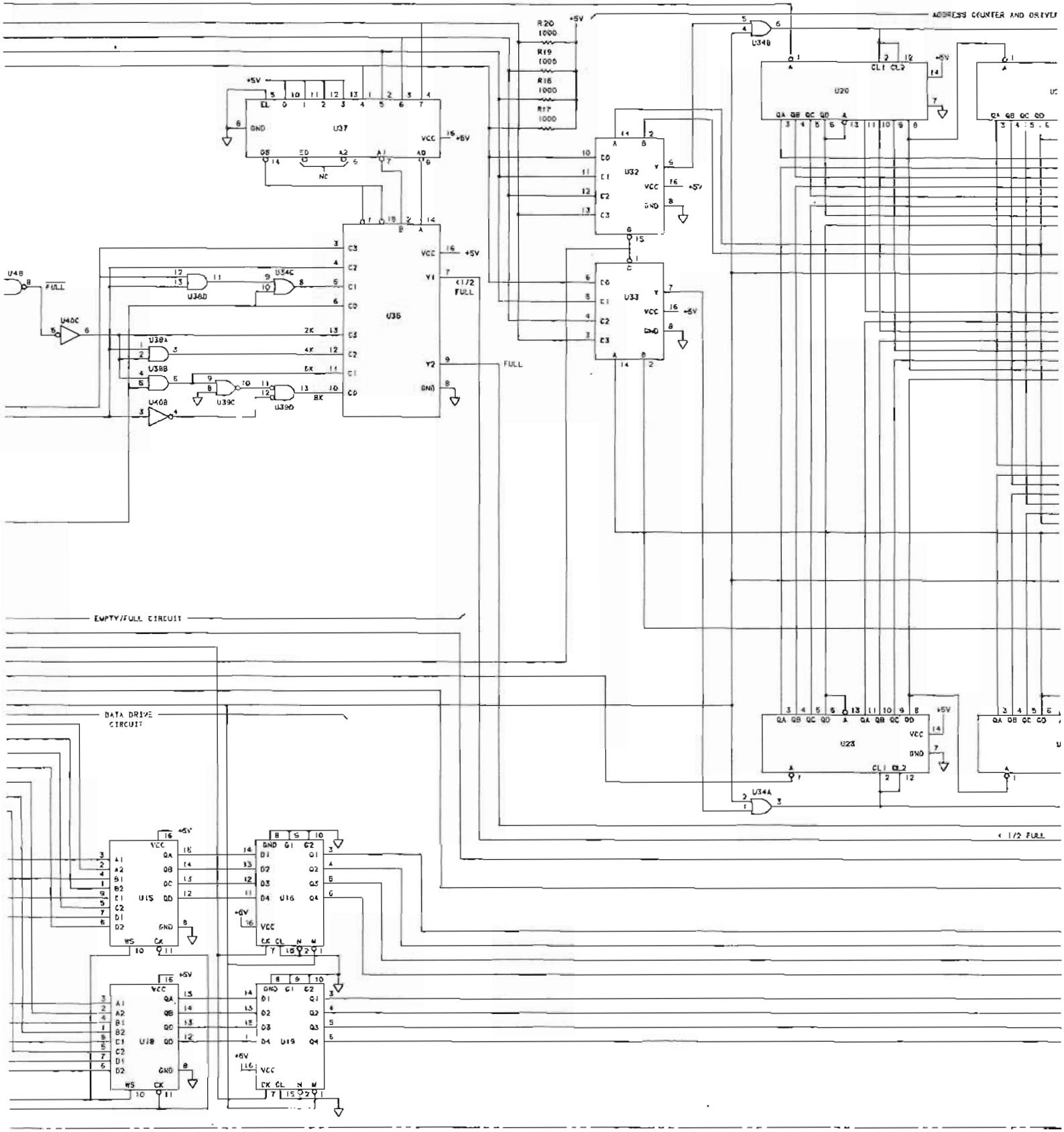
Figure 8-8. A4 Memory Control Assembly
(Sheet 1 of 2)

Figure 8-8
A4 MEMORY CONTROL ASSEMBLY
(Sheet 1 of 2)

(See Page 8-53)

A4 MEMORY CONTROL ASSEMBLY (05356-60004) SHEET 2 OF 2) SERIES 1640




ADDRESS COUNTER AND DRIVER
EMPTY/FULL CIRCUIT
DATA DRIVE CIRCUIT
R20 1000
R19 1000
R18 1000
R17 1000
+5V
U37
U36
U32
U33
U20
U23
U34A
U34B
U38A
U38B
U38C
U38D
U39C
U39D
U40A
U40B
U40C
U15
U16
U18
U19
FULL
< 1/2 FULL

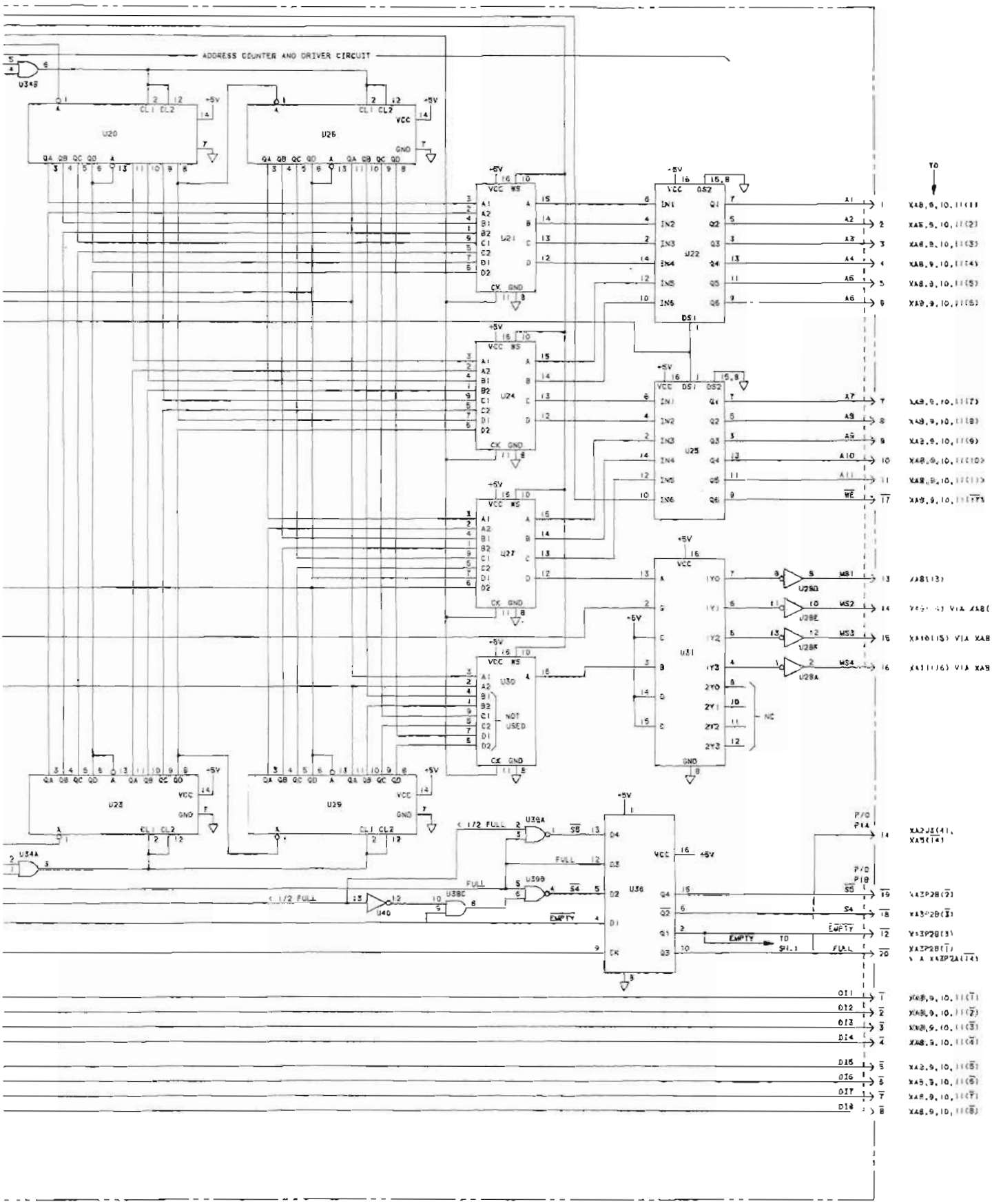
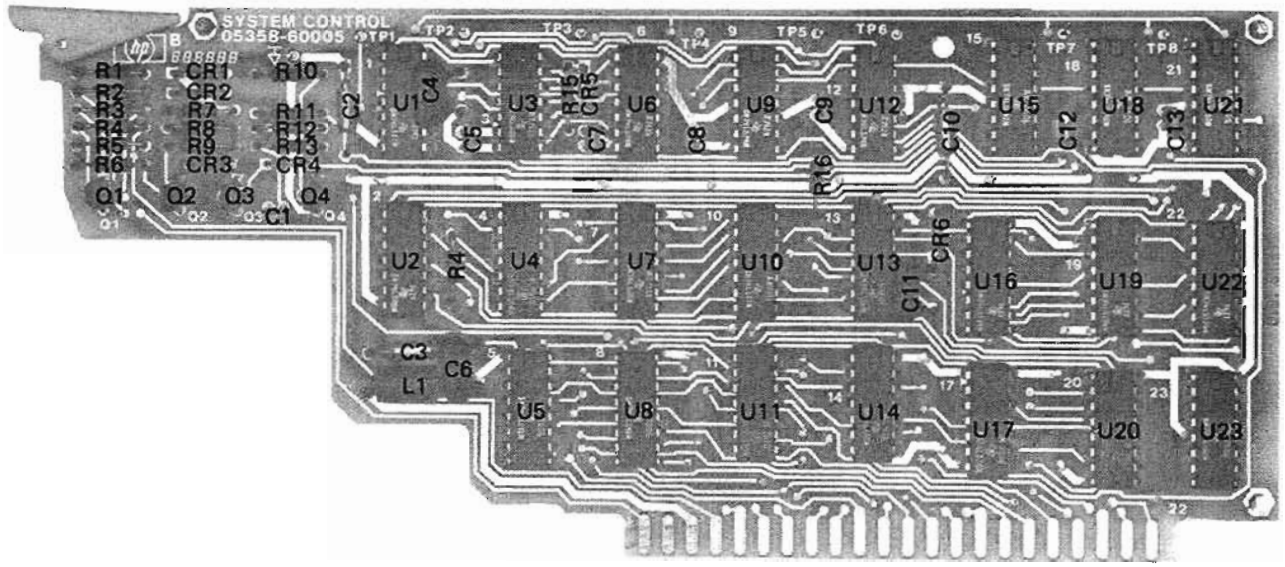


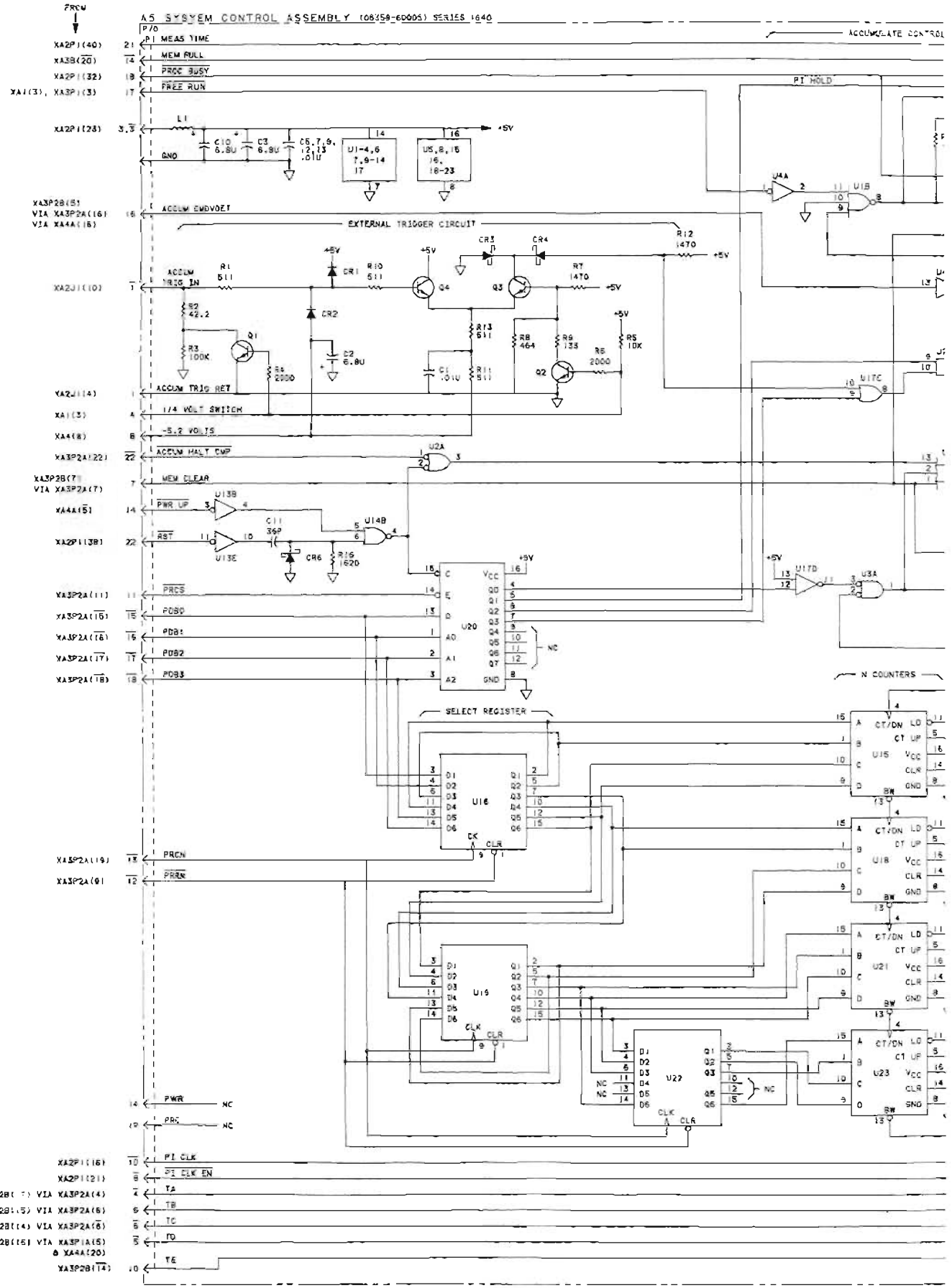
Figure 8–8. A4 Memory Control Assembly (Sheet 2 of 2)

Figure 8–8
A4 MEMORY CONTROL ASSEMBLY
(Sheet 2 of 2)

(See Page 8–55)


SYSTEM CONTROL
05358-60005
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
R1
R2
R3
R4
R5
R6
CR1
CR2
R7
R8
R9
CR3
R10
R11
R12
R13
CR4
Q1
Q2
Q3
Q4
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
L1
R4
R15
R16
CR5
CR6
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23

P1


A5 SYSYEM CONTROL ASSEMBLY (08359-60005) SERIES 1640
P/O
PRCN
PI MEAS TIME
MEM FULL
PROC BUSY
FREE RUN
PI HOLD
ACCUMULATE CONTROL
ACCUM OVDVDET
EXTERNAL TRIGGER CIRCUIT
ACCUM TRIG IN
ACCUM TRIG RET
17/4 VOLT SWITCH
-5.2 VOLTS
ACCUM HALT CMP
MEM CLEAR
PWR UP
RST
PRCS
POS0
POS1
POS2
POS3
SELECT REGISTER
N COUNTERS
PRCN
PRRN
PWR
PRC
PI CLK
PI CLK EN
TA
TB
TC
TD
TE
NC

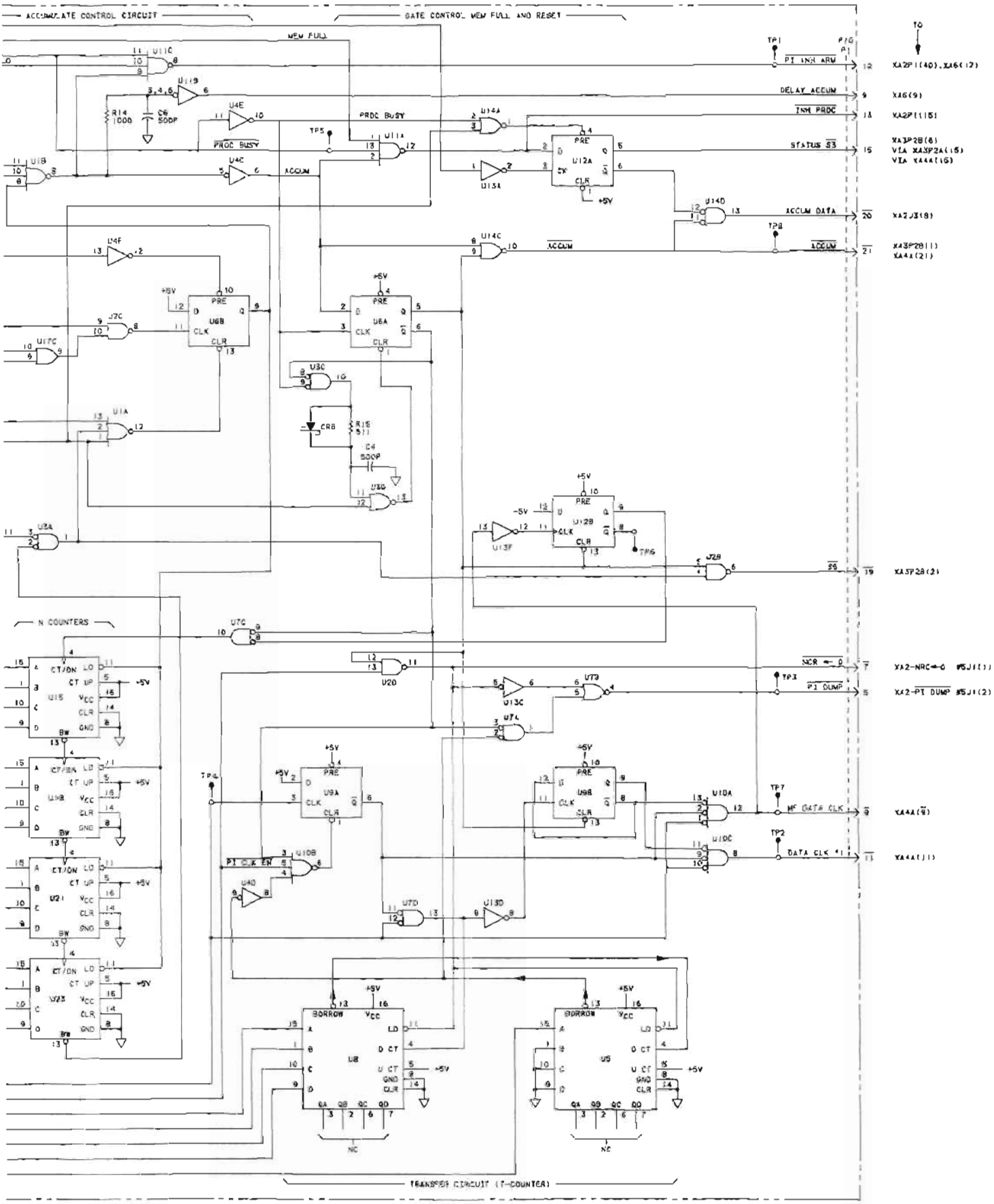
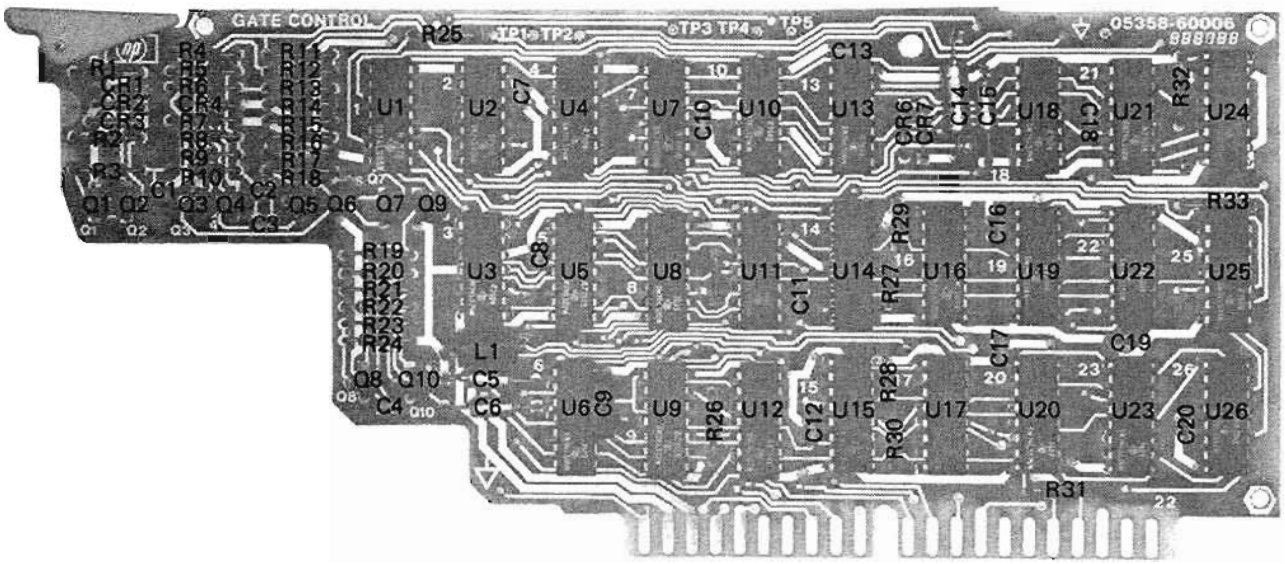


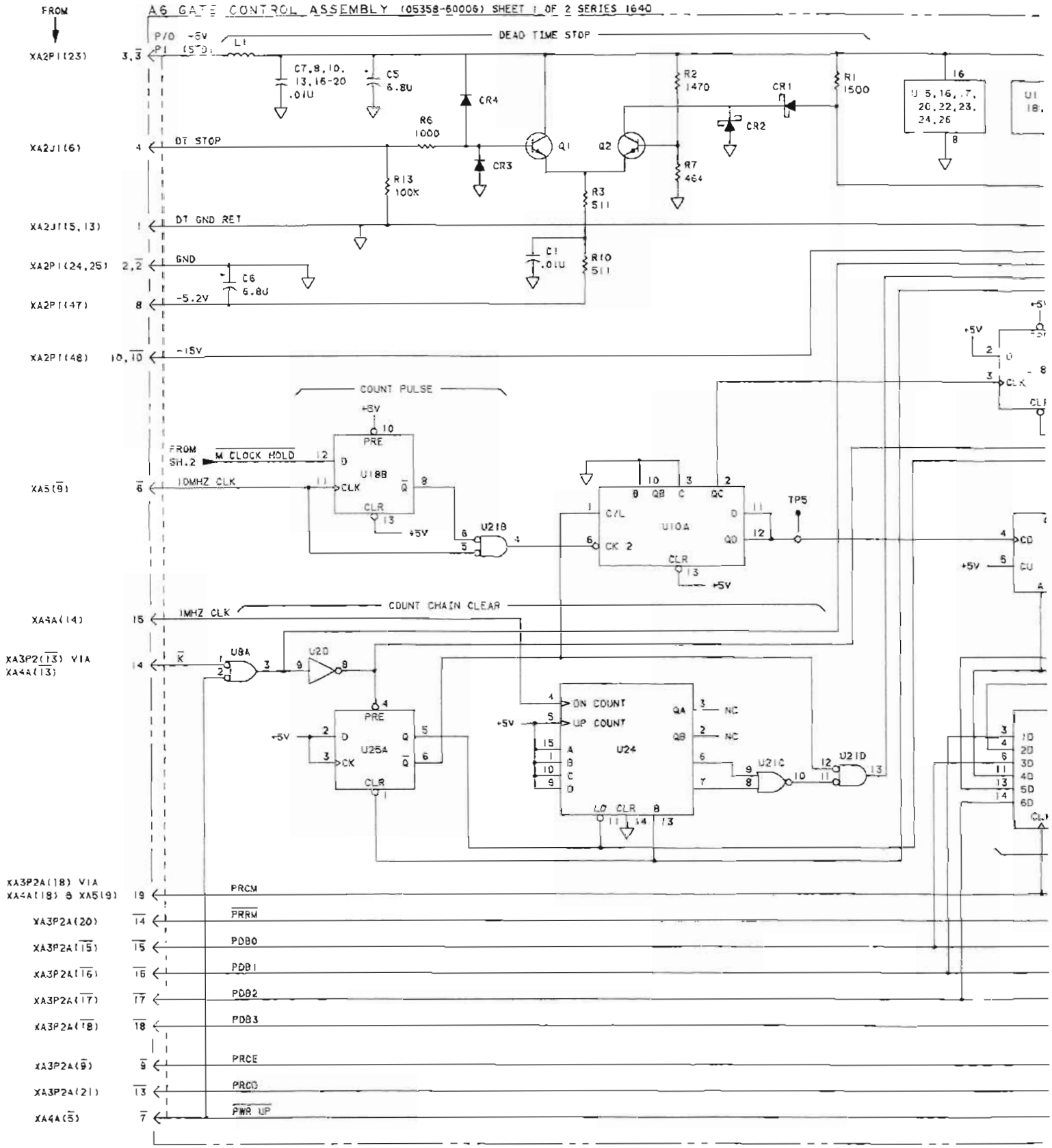
Figure 8-9. A5 System Control Assembly

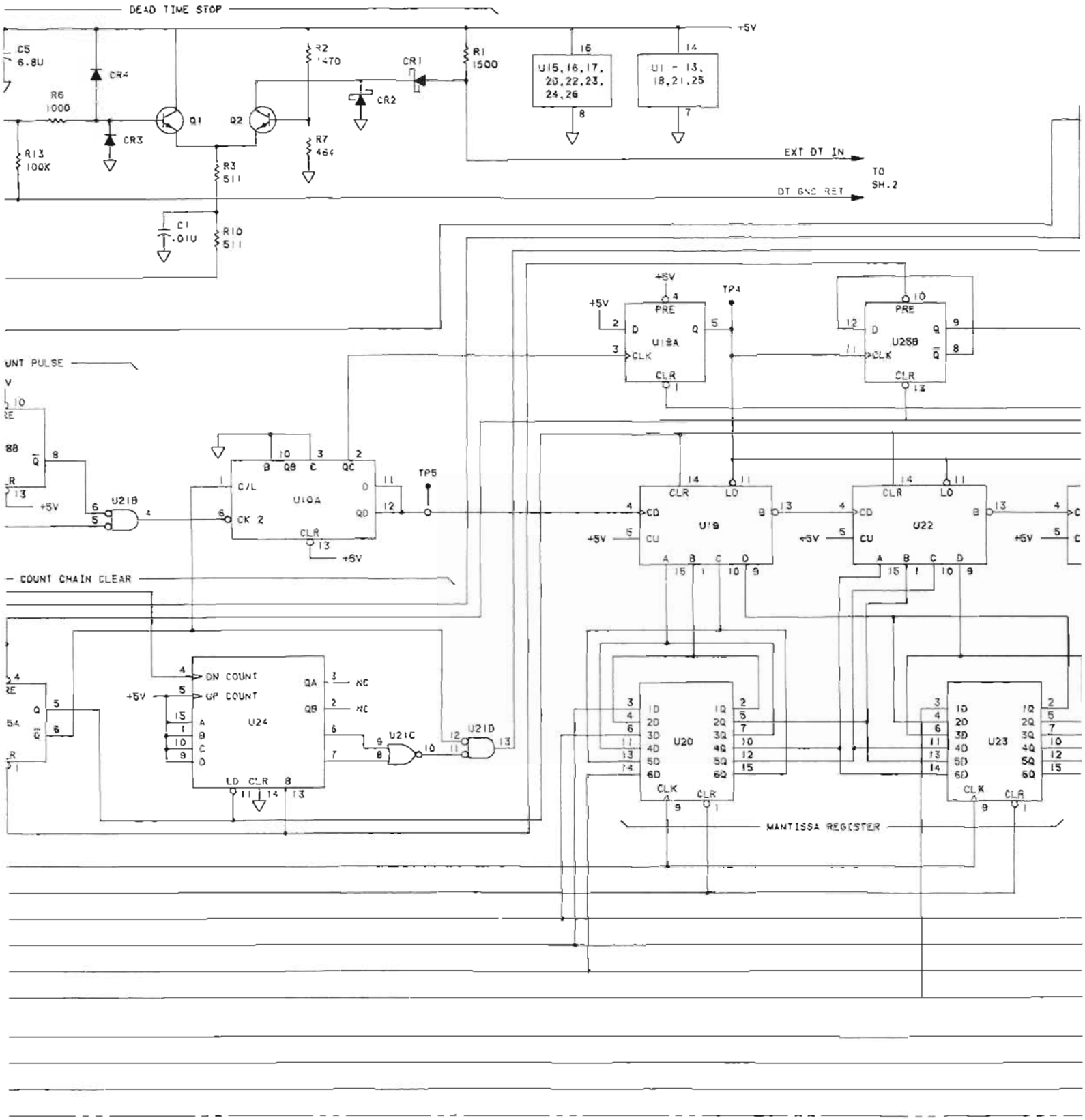
Figure 8–9
A5 SYSTEM CONTROL ASSEMBLY

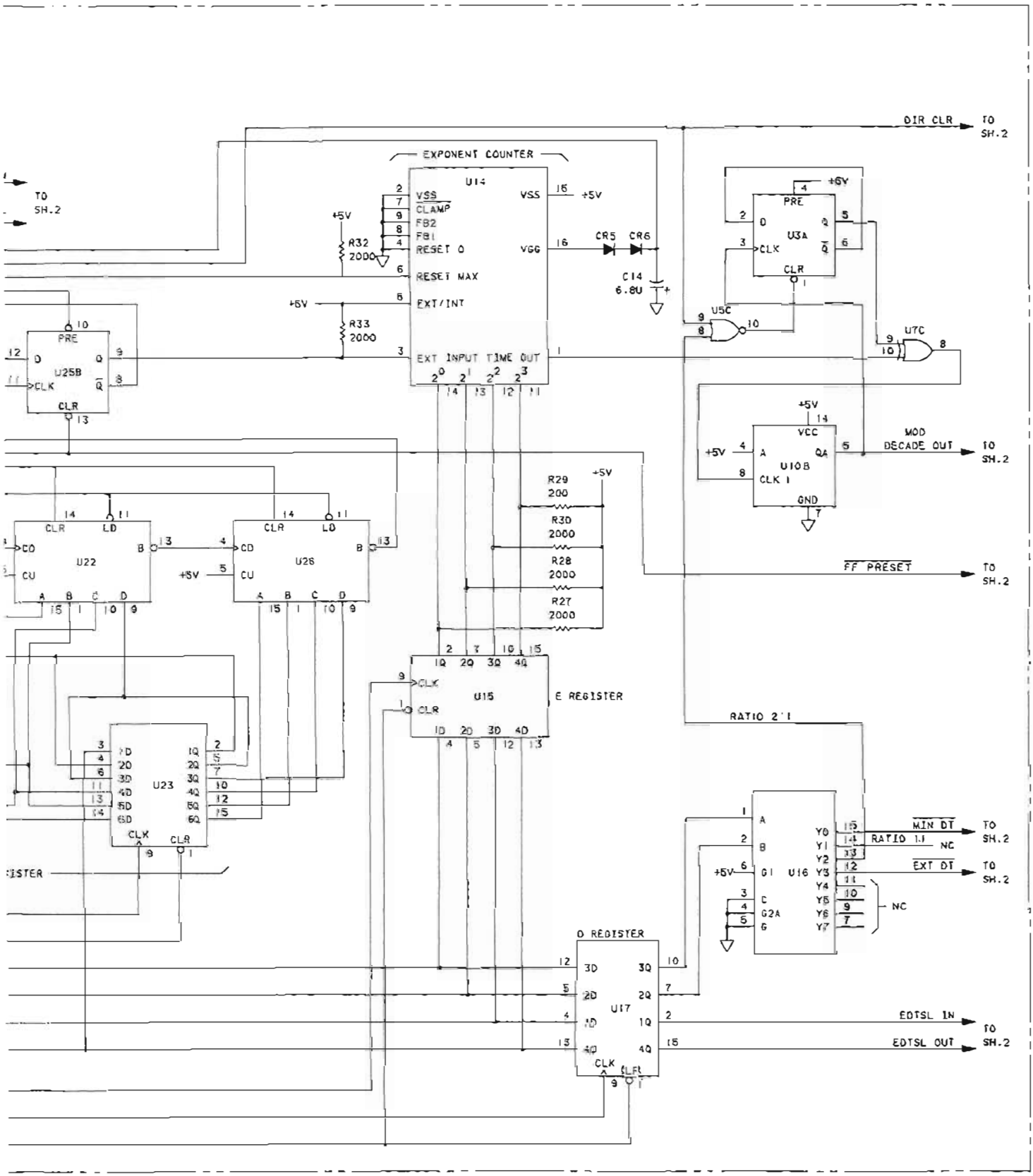
(See Page 8–57)


GATE CONTROL
05358-60006
TP1 TP2 TP3 TP4 TP5
R25
C13
U1 U2 U4 U7 U10 U13 U18 U21 U24
U3 U5 U8 U11 U14 U16 U19 U22 U25
U6 U9 U12 U15 U17 U20 U23 U26
R33
L1
C19
R31

P1


A6 GATE CONTROL ASSEMBLY (05358-60006) SHEET 1 OF 2 SERIES 1640
FROM
DEAD TIME STOP
COUNT PULSE
COUNT CHAIN CLEAR
XA2P1(23)
XA2J1(6)
XA2J1(5,13)
XA2P1(24,25)
XA2P1(47)
XA2P1(48)
XA5(9)
XA4A(14)
XA3P2(13) VIA XA4A(13)
XA3P2A(18) VIA XA4A(18) & XA5(9)
XA3P2A(20)
XA3P2A(15)
XA3P2A(16)
XA3P2A(17)
XA3P2A(18)
XA3P2A(9)
XA3P2A(21)
XA4A(5)
DT STOP
DT GND RET
GND
-5.2V
-15V
+5V
1MHZ CLK
FROM SH.2 M CLOCK HOLD
PRCM
PRRM
PDB0
PDB1
PDB2
PDB3
PRCE
PRCO
PWR UP
R1 1500
R2 1470
R3 511
R6 1000
R7 464
R10 511
R13 100K
C5 6.8U
C6 6.8U
C7,8,10, 13,16-20 .01U
C1 .01U
CR1
CR2
CR3
CR4
Q1
Q2
U188
U218
U10A
U20
U8A
U25A
U24
U21C
U21D
TP5


DEAD TIME STOP
C5 6.8U
CR4
R6 1000
CR3
R13 100K
Q1
Q2
R2 1470
CR1
CR2
R1 1500
R7 464
R3 511
C1 .01U
R10 511
U15, 16, 17, 20, 22, 23, 24, 26
U1 - 13, 18, 21, 25
+5V
EXT DT IN
TO SH. 2
DT GND RET
UNT PULSE
U18A
U28B
TP4
U21B
U10A
TP5
U19
U22
COUNT CHAIN CLEAR
U24
DN COUNT
UP COUNT
U21C
U21D
U20
U23
MANTISSA REGISTER



TEST POINTS

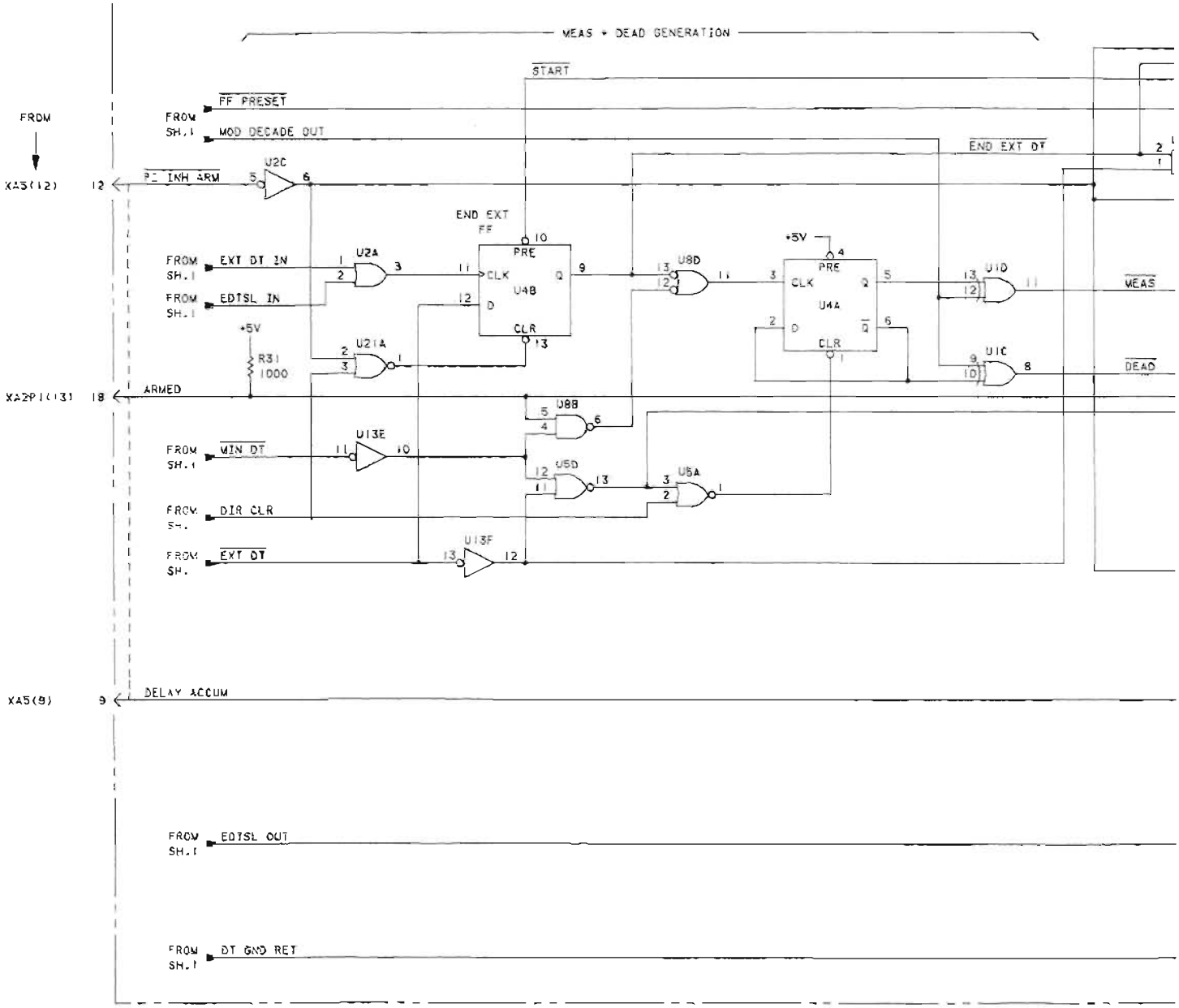
TP1	START
TP2	M CLK HOLD
TP3	MEAS
TP4	ZERO OUT
TP5	COUNT PULSE

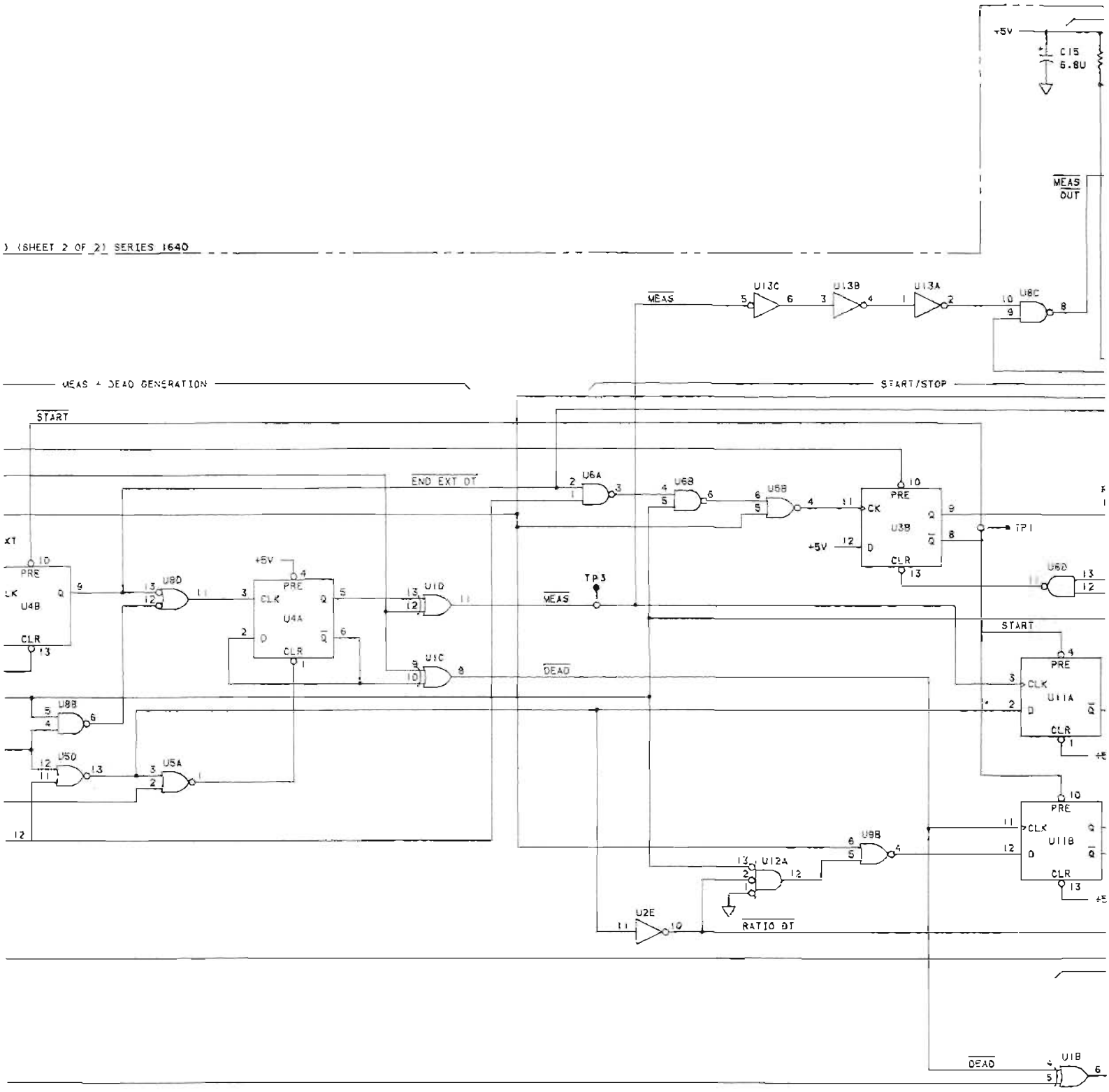
Figurre 8-10. A6 Gate Control Assembly
(Sheet 1 of 2)

Figure 8–10
A6 GATE CONTROL ASSEMBLY
(Sheet 1 of 2)

(See Page 8–59)

A6 GATE CONTROL ASSEMBLY (05358-60006) (SHEET 2 OF 2) SERIES 1840




) (SHEET 2 OF 2) SERIES 1640
+5V
C15
6.8U
MEAS
OUT
MEAS
U13C
U13B
U13A
U8C
MEAS & DEAD GENERATION
START/STOP
START
END EXT DT
U6A
U6B
U6B
U8B
PRE
CK
D
CLR
U3B
TP1
+5V
U6D
TP3
MEAS
START
U8D
U4B
U4A
U1D
U1C
DEAD
U11A
U8B
U5D
U5A
U11B
U9B
U12A
U2E
RATIO DT
DEAD
U1B

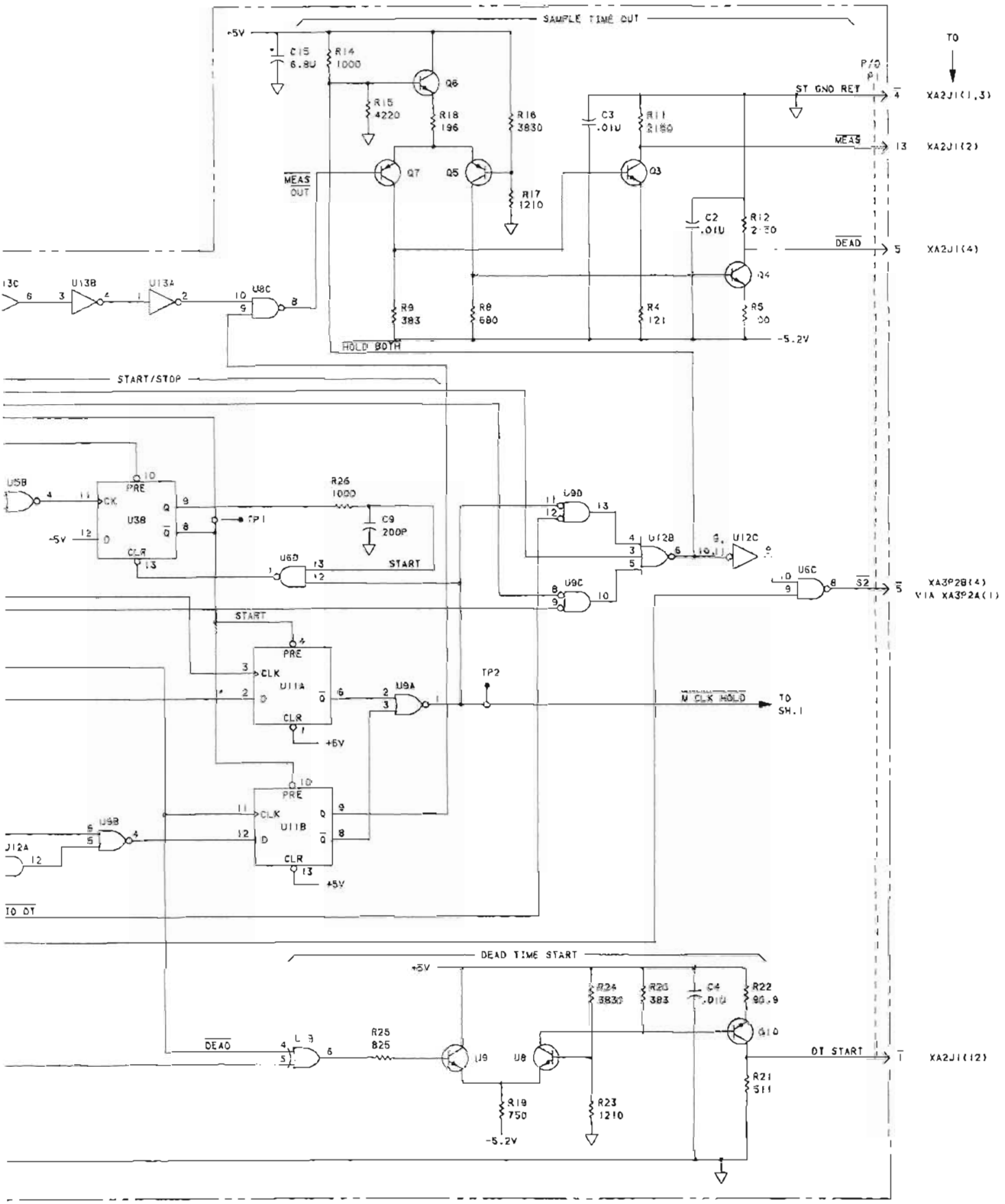
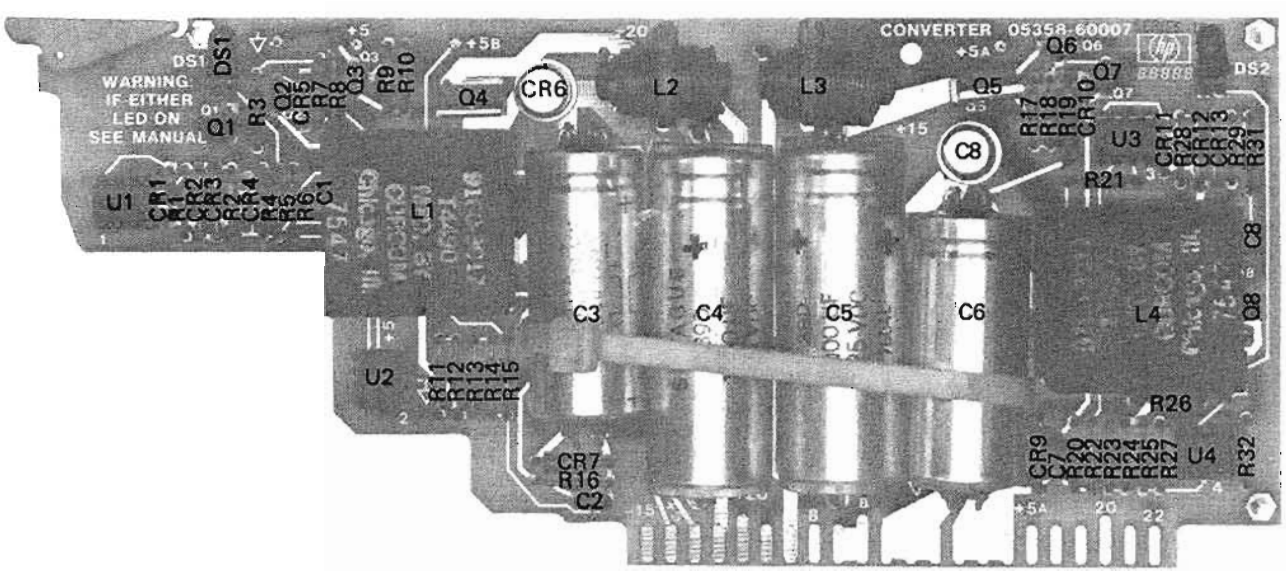
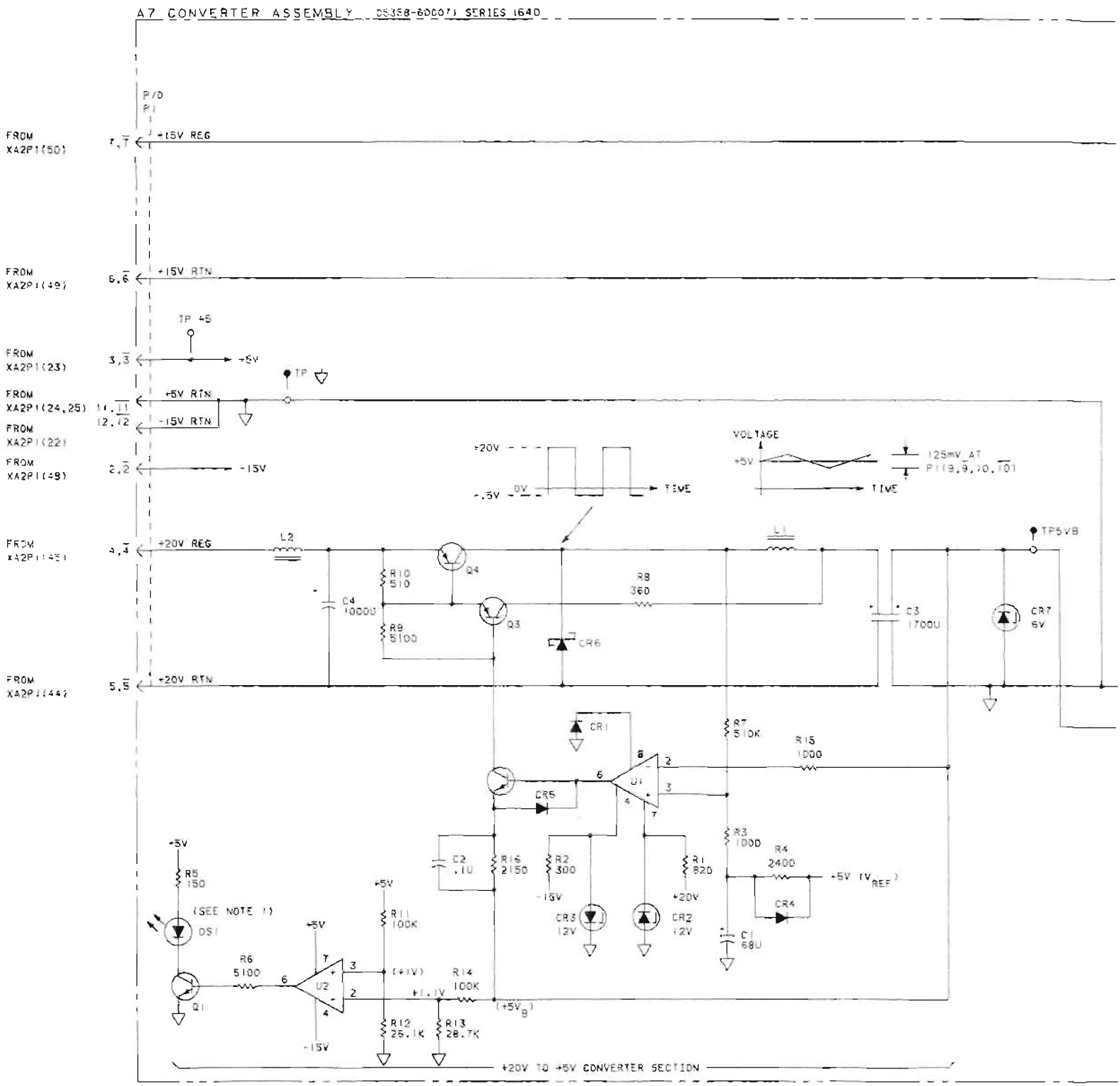


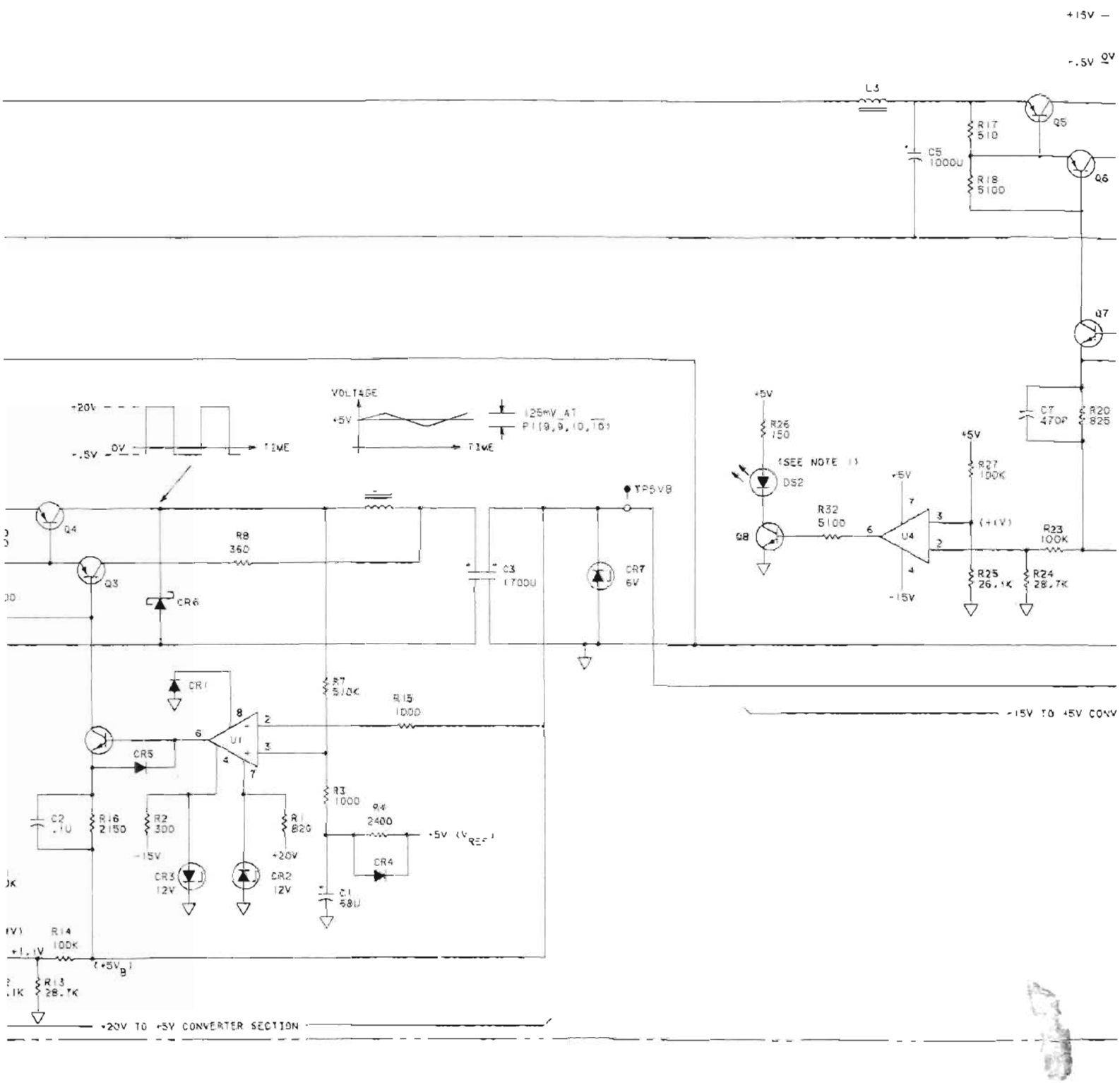
Figure 8-10. A6 Gate Control Assembly (Sheet 2 of 2)

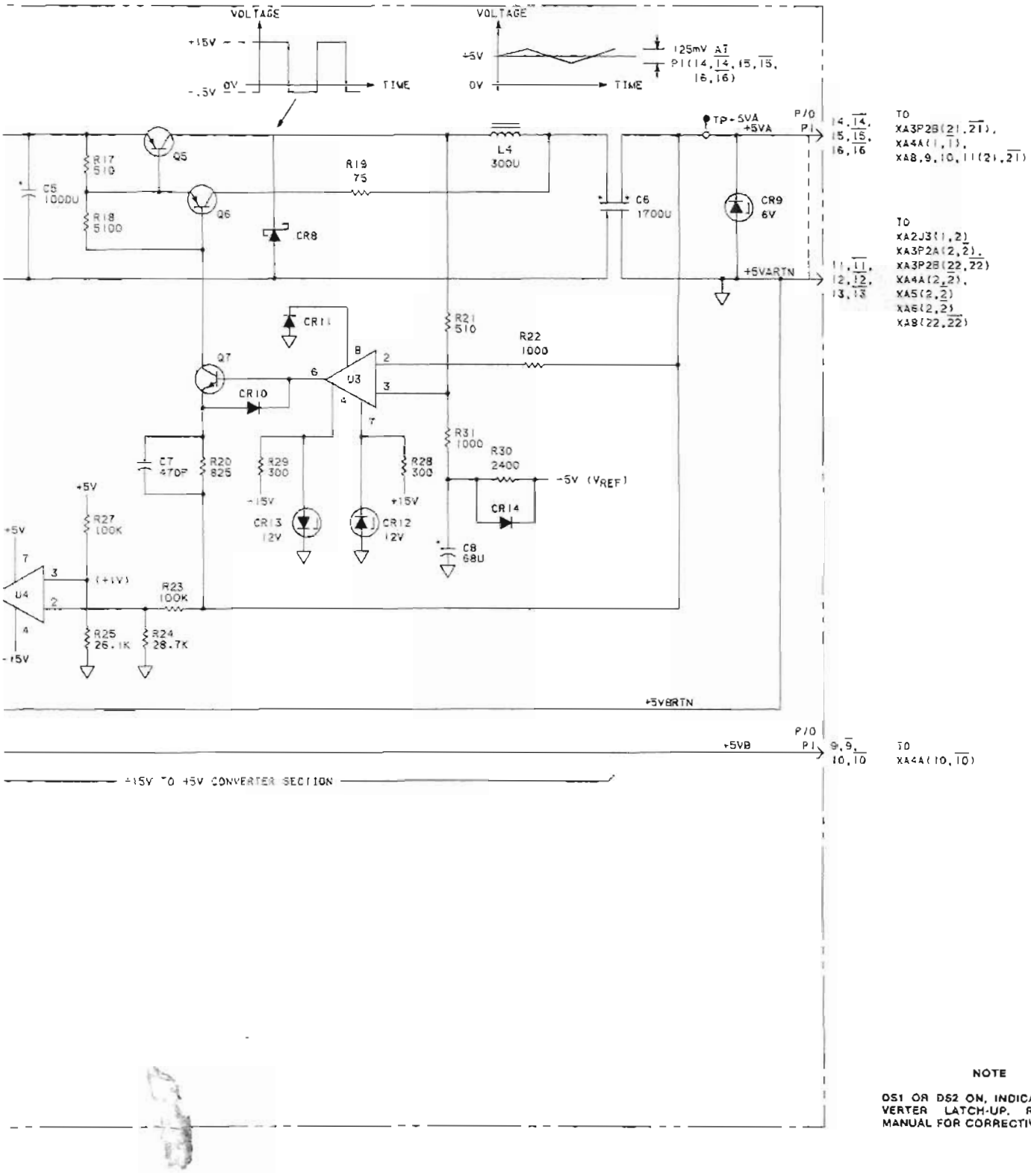
Figure 8–10
A6 GATE CONTROL ASSEMBLY
(Sheet 2 of 2)

(See Page 8–61)


CONVERTER 05358-60007
WARNING
IF EITHER
LED ON
SEE MANUAL
DS1
DS2
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CR6
L1
L2
L3
L4
C3
C4
C5
C6
C8
U1
U2
U3
U4
R21
R26
CR7
R16
C2


A7 CONVERTER ASSEMBLY 05368-60007) SERIES 1640
P/O P1
FROM XA2P1(50)
7,7
+15V REG
FROM XA2P1(49)
6,6
+15V RTN
TP 45
FROM XA2P1(23)
3,3
+5V
TP
FROM XA2P1(24,25)
11,11
12,12
+5V RTN
-15V RTN
FROM XA2P1(22)
FROM XA2P1(48)
2,2
-15V
+20V
-.3V
0V
TIME
VOLTAGE
+5V
125mV AT P1(8,9,10,10)
TIME
FROM XA2P1(45)
4,4
+20V REG
L2
L1
TP5VB
R10 510
Q4
R8 360
C4 1000U
R9 5100
Q3
CR6
C3 1700U
CR7 6V
FROM XA2P1(44)
5,5
+20V RTN
CR1
R7 510K
R15 1000
U1
CR5
R3 1000
R4 2400
+5V (VREF)
C2 .1U
R16 2150
R2 300
R1 820
-15V
+20V
CR3 12V
CR2 12V
CR4
C1 68U
+5V
R5 150
(SEE NOTE 1)
DS1
+5V
R11 100K
R6 5100
U2
(+1V)
R14 100K
+1.1V
(+5VB)
Q1
R12 28.1K
R13 28.7K
-15V
+20V TO +5V CONVERTER SECTION


+15V
-.5V
0V
L3
C5
1000U
R17
510
Q5
R18
5100
Q6
Q7
C7
470P
R20
825
+20V
-.5V
0V
TIME
VOLTAGE
+5V
125mV AT
P(10,9,10,T6)
TIME
+5V
R26
150
(SEE NOTE 1)
DS2
Q8
R32
5100
U4
R27
100K
(+1V)
R23
100K
R25
26.1K
R24
28.7K
-15V
TP5VB
Q4
Q3
R8
360
CR6
C3
1700U
CR7
6V
CR1
R7
510K
R15
1000
U1
CR5
C2
.1U
R16
2150
R2
300
R1
820
R3
1000
R4
2400
+5V (VREF)
-15V
+20V
CR3
12V
CR2
12V
CR4
C1
68U
R14
100K
(+5VB)
R13
28.7K
-15V TO +5V CONV
+20V TO +5V CONVERTER SECTION



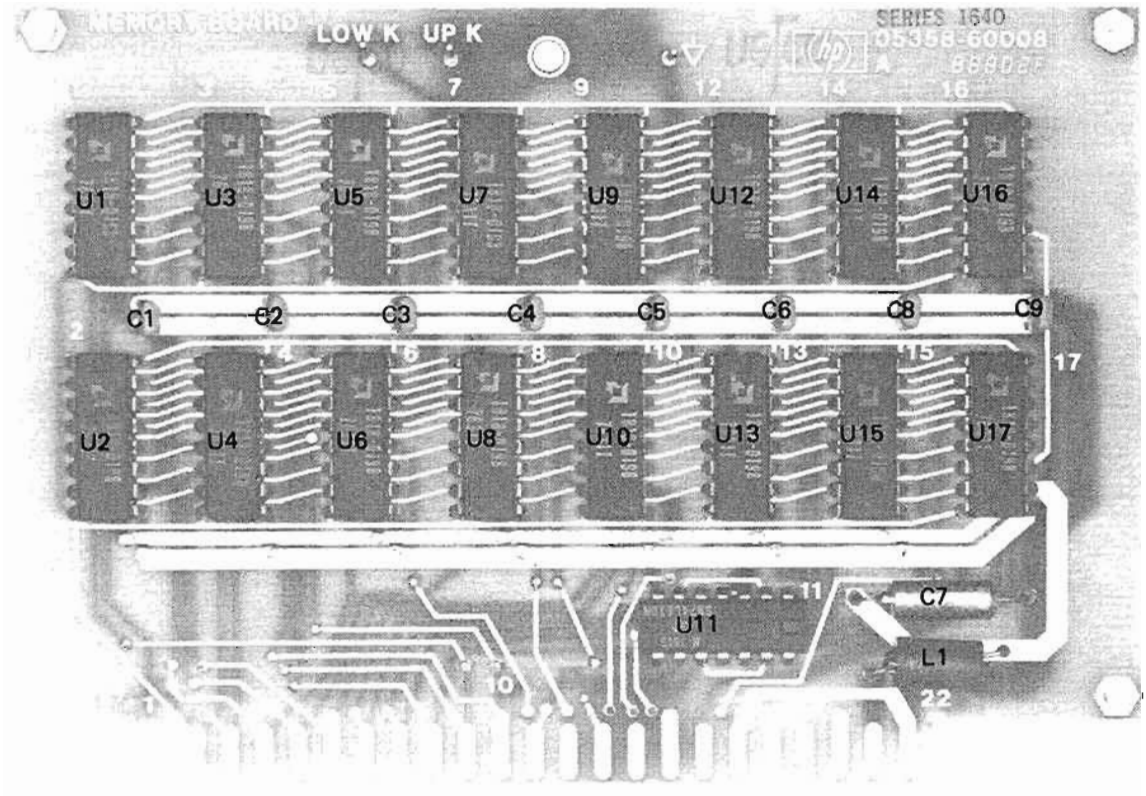
NOTE

DS1 OR DS2 ON, INDICATES CONVERTER LATCH-UP. REFER TO MANUAL FOR CORRECTIVE ACTION.

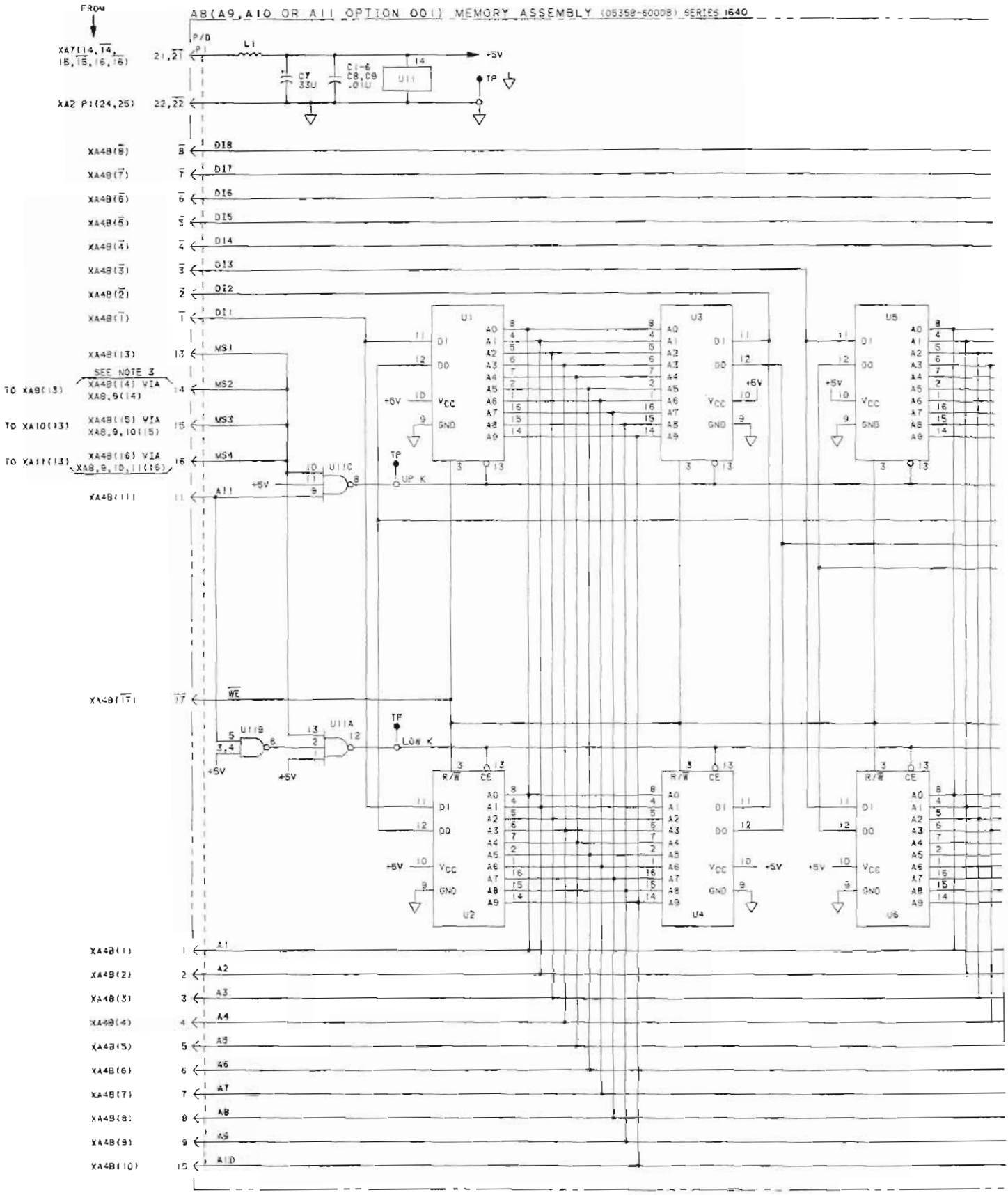
Figure 8-11. A7 Converter Assembly

Figure 8-11
A7 CONVERTER ASSEMBLY

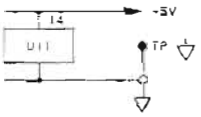
(See Page 8–63)

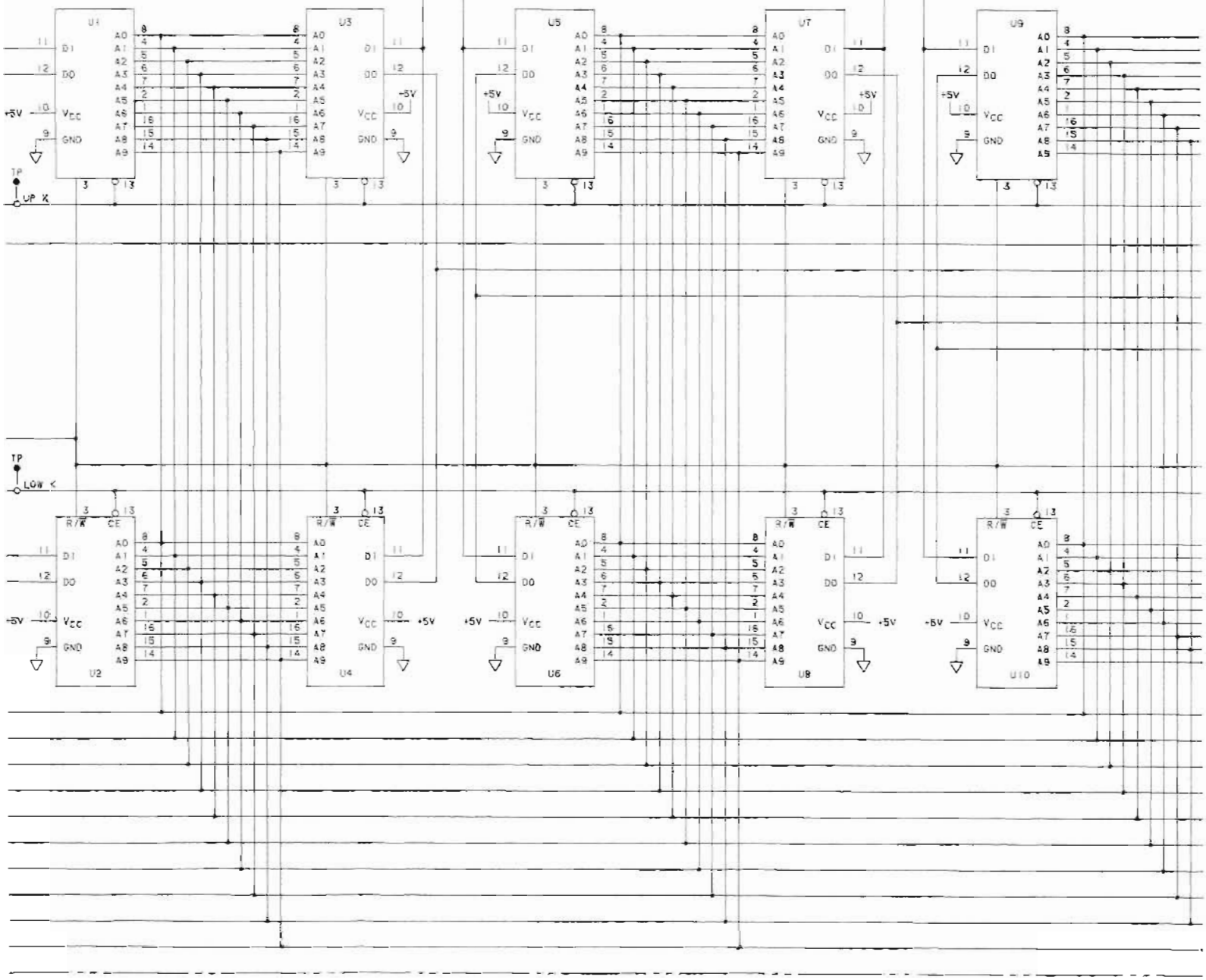

LOW K
UP K
SERIES 1640
05358-60008
U1
U3
U5
U7
U9
U12
U14
U16
C1
C2
C3
C4
C5
C6
C8
C9
U2
U4
U6
U8
U10
U13
U15
U17
U11
C7
L1

P1


A8(A9,A10 OR A11 OPTION 001) MEMORY ASSEMBLY (05358-60008) SERIES 1640
FROM
P/O P1
L1
+5V
C7 33U
C1-6 C8,C9 .01U
U11
TP
XA7(14,14, 15,15,16,16)
21,21
XA2 P1(24,25)
22,22
XA4B(8) 8 DI8
XA4B(7) 7 DI7
XA4B(6) 6 DI6
XA4B(5) 5 DI5
XA4B(4) 4 DI4
XA4B(3) 3 DI3
XA4B(2) 2 DI2
XA4B(1) 1 DI1
XA4B(13) 13 MS1
SEE NOTE 3
TO XA9(13) XA4B(14) VIA XA8,9(14) 14 MS2
TO XA10(13) XA4B(15) VIA XA8,9,10(15) 15 MS3
TO XA11(13) XA4B(16) VIA XA8,9,10,11(16) 16 MS4
XA4B(11) 11 A11
XA4B(17) 17 WE
XA4B(1) 1 A1
XA4B(2) 2 A2
XA4B(3) 3 A3
XA4B(4) 4 A4
XA4B(5) 5 A5
XA4B(6) 6 A6
XA4B(7) 7 A7
XA4B(8) 8 A8
XA4B(9) 9 A9
XA4B(10) 10 A10
U1
U2
U3
U4
U5
U6
U11A
U11B
U11C
UP K
LOW K
TP
+5V
VCC
GND
R/W
CE
DI
DO
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9

ON 0011 MEMORY ASSEMBLY (05358-60008) SERIES 1640





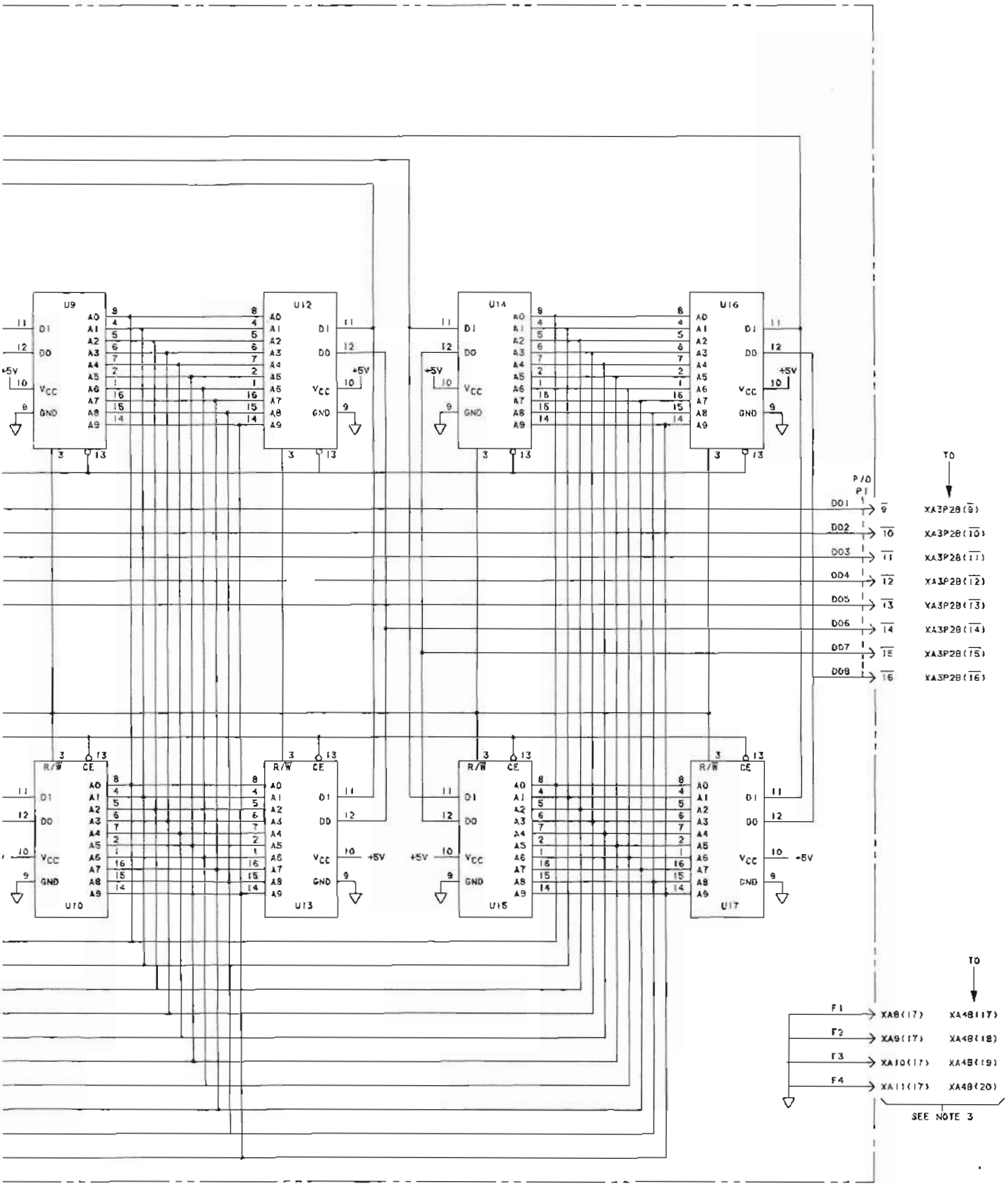
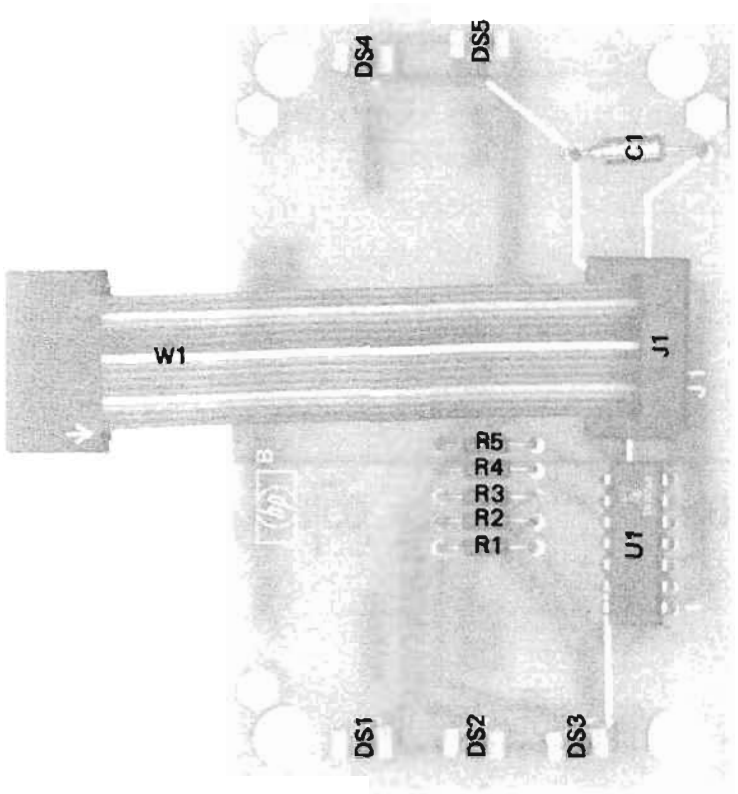


Figure 8-12. A8 (or Optional A9, A10, A11) Memory Assembly

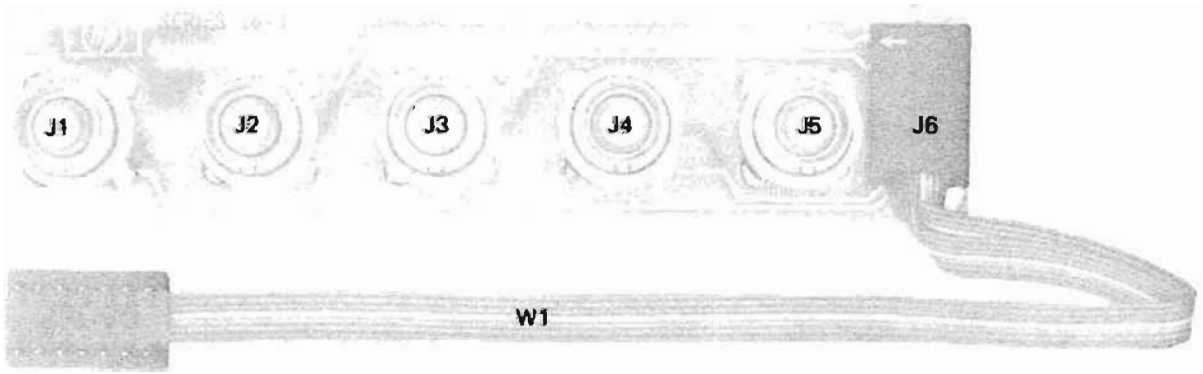
Figure 8–12
A8 (OR OPTIONAL A9, A10, A11) MEMORY ASSEMBLY

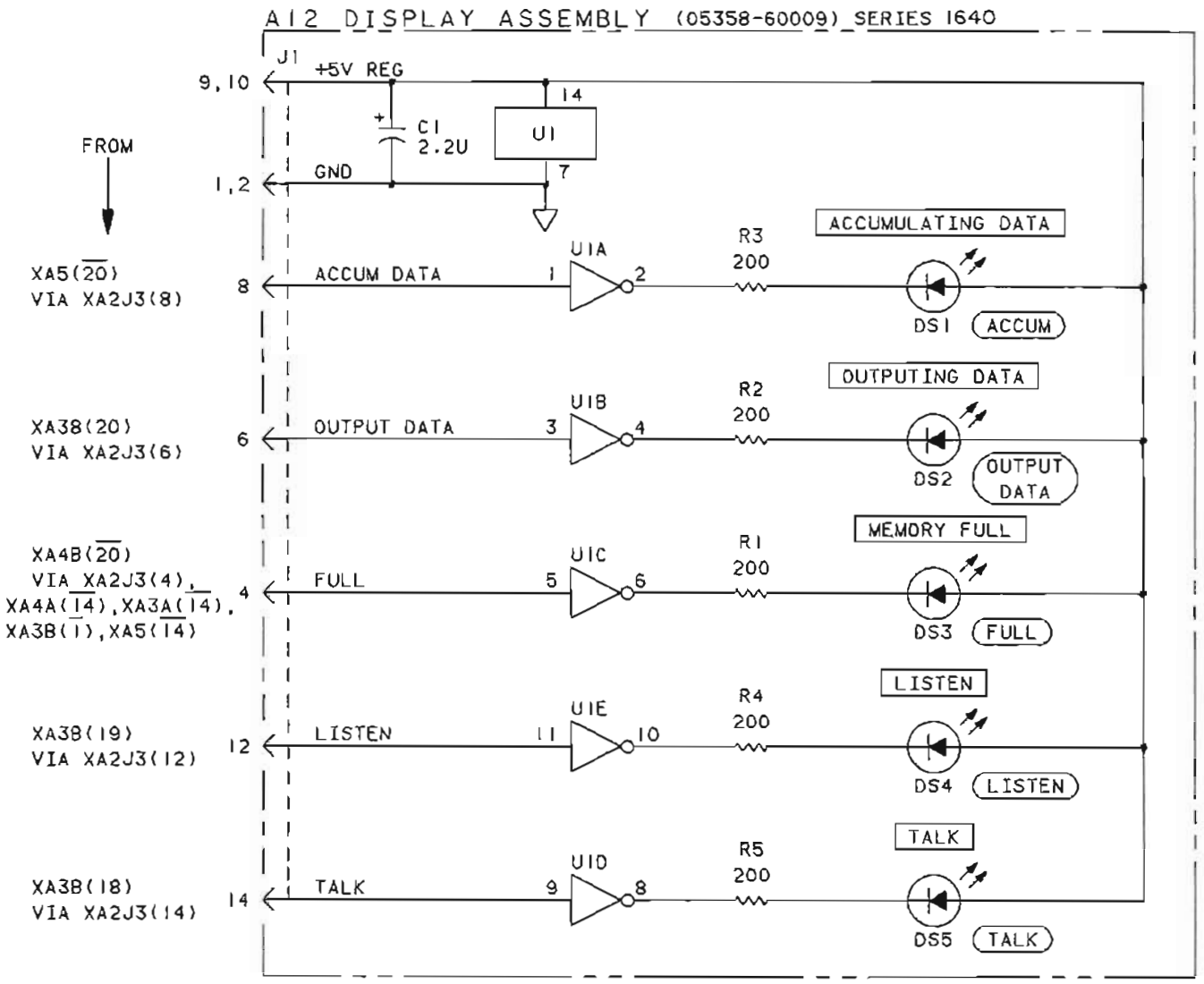
(See Page 8–65)

A12



A13




A12 DISPLAY ASSEMBLY (05358-60009) SERIES 1640
J1
9,10
+5V REG
14
C1
2.2U
U1
GND
1,2
7
FROM
XA5(20)
VIA XA2J3(8)
8
ACCUM DATA
U1A
1
2
R3
200
ACCUMULATING DATA
DS1
ACCUM
XA38(20)
VIA XA2J3(6)
6
OUTPUT DATA
U1B
3
4
R2
200
OUTPUTING DATA
DS2
OUTPUT DATA
XA4B(20)
VIA XA2J3(4),
XA4A(14),XA3A(14),
XA3B(1),XA5(14)
4
FULL
U1C
5
6
R1
200
MEMORY FULL
DS3
FULL
XA38(19)
VIA XA2J3(12)
12
LISTEN
U1E
11
10
R4
200
LISTEN
DS4
LISTEN
XA3B(18)
VIA XA2J3(14)
14
TALK
U1D
9
8
R5
200
TALK
DS5
TALK

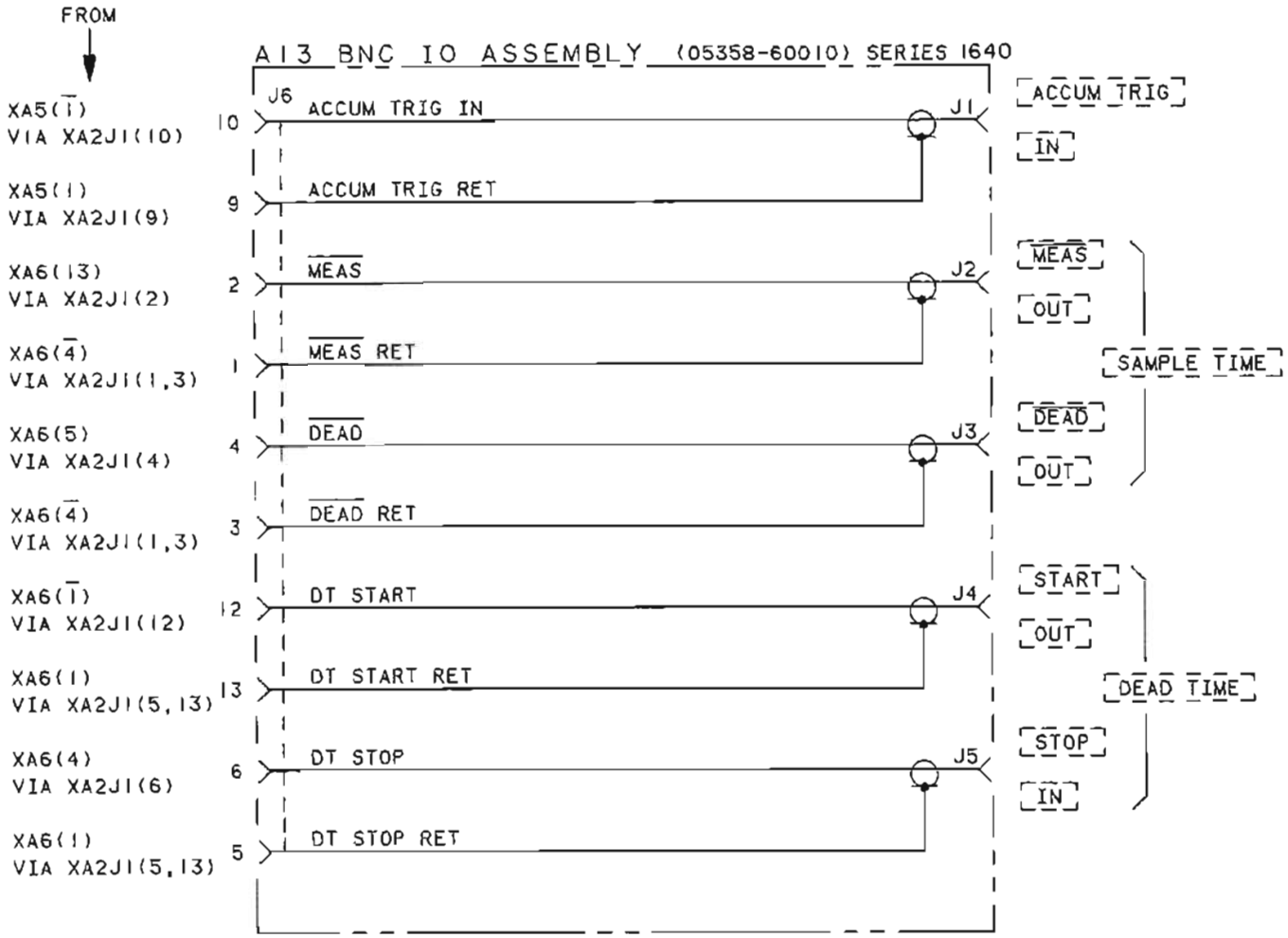


Figure 8-13. A12 Display Assembly and A13 BNC I/O Assembly

Figure 8-13
A12 DISPLAY ASSEMBLY AND
A13 BNC I/O ASSEMBLY

(See Page 8-67)

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