HP 11835A Data Buffer
Option 001- GSM
Option 002 - NADC, JDC

Technical Data

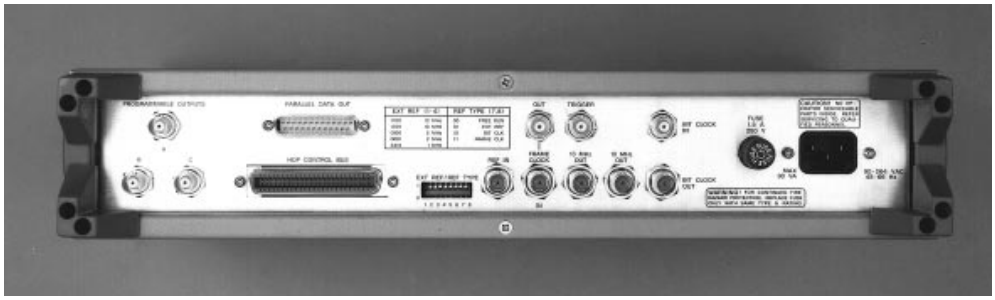
The HP 11835A Data Buffer with HP 8657A Option 001

Configurable buffer designed to provide a programmable, serial bit stream and clock.

The HP 11835A Data Buffer is designed to be a configurable data output device. Its primary function is to buffer data from a computer, and output the data as a serial bit stream. The HP 11835A can output this serial data at any rate from dc to approximately 4 MHz with a user supplied bit clock. Optionally, an internal reference board will provide the bit clock used by the GSM digital cellular system (Option 001), or the bit or symbol clock used in the North American Digital Cellular System and the Japanese Digital Cellular System (Option 002).

In addition, the HP 11835A has a large memory which can be configured as a programmable state machine, allowing it to support digital mobile radio applications utilizing TDMA techniques. The HP 11835A also can drive a fast-hopping signal generator such as the HP 8662A-H25 to simulate frequency hopping. Flexibility and configurability make the HP 11835A the perfect choice for testing new digital mobile communication systems.

Data is downloaded to the HP 11835A via the included GPIO cable (General Purpose Input output) from an external controller (HP 9000 Series 300 with GPIO interface card). The data for the active timeslot(s) is stored in a large first-in, first-out (FIFO) RAM memory. The FIFO memory consists of two banks each having a capacity of 1.024 Mbits. The FIFO memory can be loaded from GPIO while the active data is clocked out. This allows the HP 11835A to continuously output changing data during the active timeslot(s) to simulate radio transmissions. In addition to the FIFO memory, there is a 128K x 16 bit frame control RAM. This memory essentially implements a state machine which controls the operation of the HP 11835A. The frame control RAM outputs data (stored during configuration) during inactive timeslot(s), clocks the memory (64K x 8 bit) used for the Hop Control Bus, and selects the FIFO output as the data source during the active timeslot(s). Three additional frame control RAM outputs are available on the rear-panel as programmable outputs with bit period resolution.



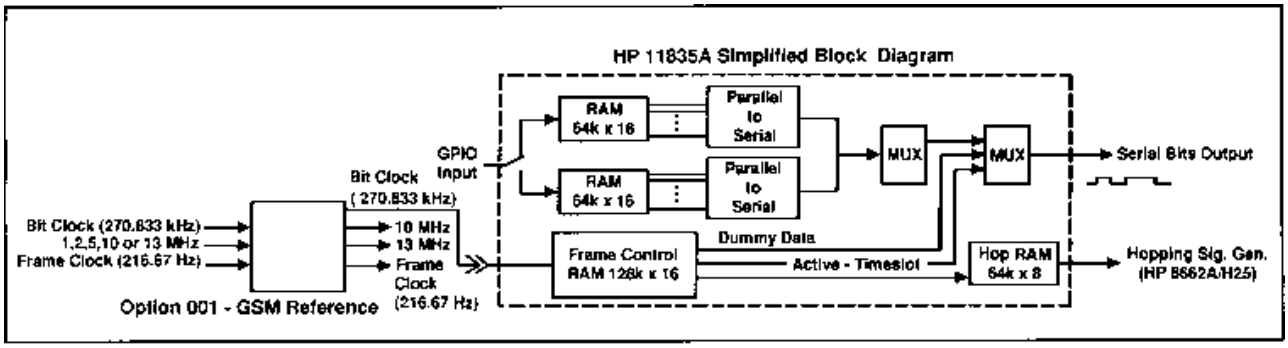
Rear panel of HP 11835A with Option 002

Option 001 GSM Reference

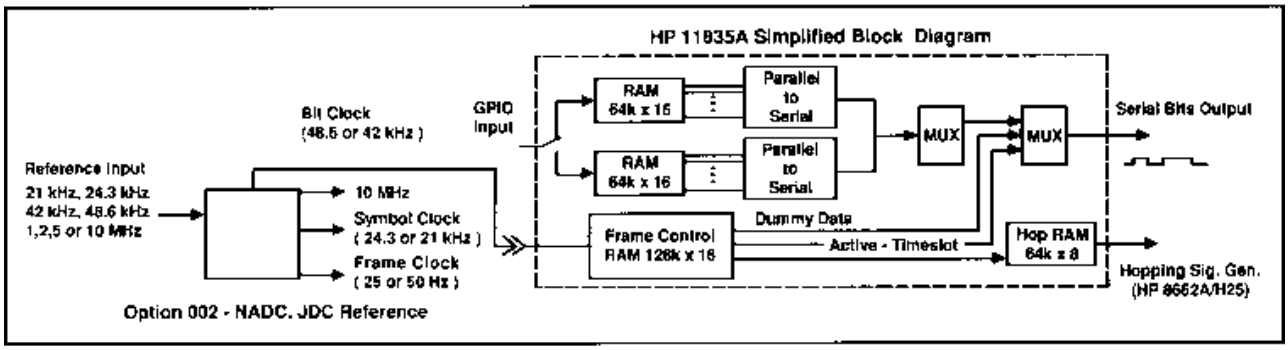
Option 001 GSM reference provides synchronization of the HP 11835A with the clock frequencies used by the Pan-European Digital Cellular Radio System. This option permits the use of 1, 2, 5, or 10 MHz instrumentation references, 216.67 Hz (frame clock), 270.833 kHz (bit clock), or 13 MHz GSM clocks as reference inputs. From these inputs 10 MHz, 13 MHz, 270.833 kHz (hit clock) and 216.67 Hz (frame clock) signals are generated and output. These signals permit test instrumentation and GSM transceivers to be synchronized for accurate, repeatable measurements. Option 001 also, simplifies locking other test equipment to GSM clock frequencies by providing a 10 MHz output which is phase locked to GSM frame clock, bit clock, or 13 MHz.

Option 002 NADC, JDC Reference

Option 002 NADC, JDC reference provides similar capabilities as the Option 001 GSM reference, but for either the North American Digital Cellular System or the Japanese Digital Cellular System. When configured for the NADC system, the HP 11835A Option 002 can use 1, 2, 5, or 10 MHz instrumentation references, 48.6 kHz (bit clock), or 24.3 kHz (symbol clock) as reference inputs. Option 002 also provides NADC frame clock (25 Hz), bit clock (48.6 kHz), and symbol clock (24.3 kHz) outputs. When configured for the JDC system, Option 002 provides the same inputs and outputs, but uses the Japanese systems' frequencies. These include bit clock (42 kHz), symbol clock (21 kHz), and frame clock (50 Hz).



HP 11835A Option 001 Simplified block diagram



HP 11835A Option 002 Simplified block diagram

HP 11835A SPECIFICATIONS

Inputs (TTL levels)
Bit Clock Input: BNC, rear-panel.
GPIO Input: 50-pin, front-panel.
Trigger Input: BNC, rear-panel.

Outputs (TTL levels)
Data Output: BNC, front-panel.
Clock Output: BNC, front-panel.
Program Outputs: 25-pin, front-panel.
Parallel Bus Output: 25-pin, rear-panel.
Hop Control Bus: 50-pin, rear-panel.
Programmable Outputs: 3 BNCs, rear-panel.

Option 001 Specifications

Option 001 adds a reference board to generate the required bit clock (270.833 kHz) for use in the GSM digital cellular system.

Reference Modes: Reference Lock, Bit Clock Lock, Frame Clock Lock, or Free Run.
Inputs: (rear panel BNCs)
Reference: 1, 2, 5, 10, 13 MHz, >0 dBm (50Q nominal).
Frame Clock: 216.67 Hz, TTL levels.
Bit Clock: 270.833 kHz, TTL levels.
Outputs: (rear panel BNCs) 10 MHz, 13 MHz, 270.833 kHz (Bit Clock), 216.67 Hz (Frame Clock)

Option 002 Specifications

Option 002 adds a reference board to generate the required symbol or bit clocks for use in the NADC (North American Digital Cellular) system or the JDC (Japanese Digital Cellular) system.

Reference Modes: Reference Lock, Bit Clock Lock, Symbol Clock Lock, or Free Run.
Reference Input (rear panel BNC): accepts 21 kHz, 24.3 kHz, 42 kHz, 48.6 kHz at TTL levels or 1 MHz, 2 MHz, 5 MHz, or 10 MHz into 50Q.
Outputs (rear panel BNCs):
Reference: 10 MHz (50Q nominal).
Symbol Clock: 24.3 kHz or 21 kHz, TTL levels.
Bit Clock: 48.6 kHz or 42 kHz, TTL levels.
Frame Clock: 25 Hz or 50 Hz, TTL levels.

General

Operating Temperature Range: 0° to +55°C.
Storage Temperature Range: -55° to +75° C.
Power Requirements: 90 to 264 volts from 48 to 66 Hz; 75 VA maximum. Weight: Net 6 kg (14 lb); shipping 11 kg (24 Ib).
Dimensions: 88.1H x 425W x 346D mm. (3.5 x 16.75 x 13.6 inches).
Cables: includes GPIO cable to connect HP 11835A to host computer and a ribbon cable to connect the HP 11835A to a HP 8662-H25 Fast-Hop Signal Generator.

Ordering Information

HP 11835A Data Buffer
Option 001 - GSM Reference*
Option 002 - NADC/JDC Reference*
*Only one option can be ordered

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Hong Kong
Fax: (852) 2506 9285

Printed in U.S.A. 12/96
5091-1239E